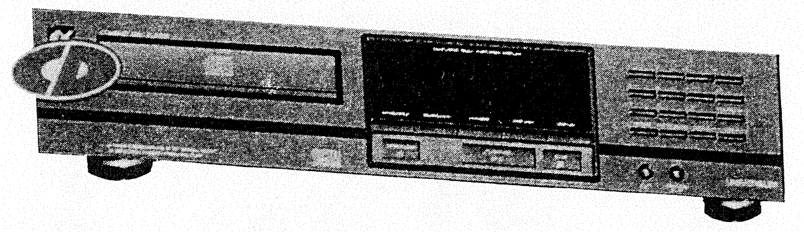
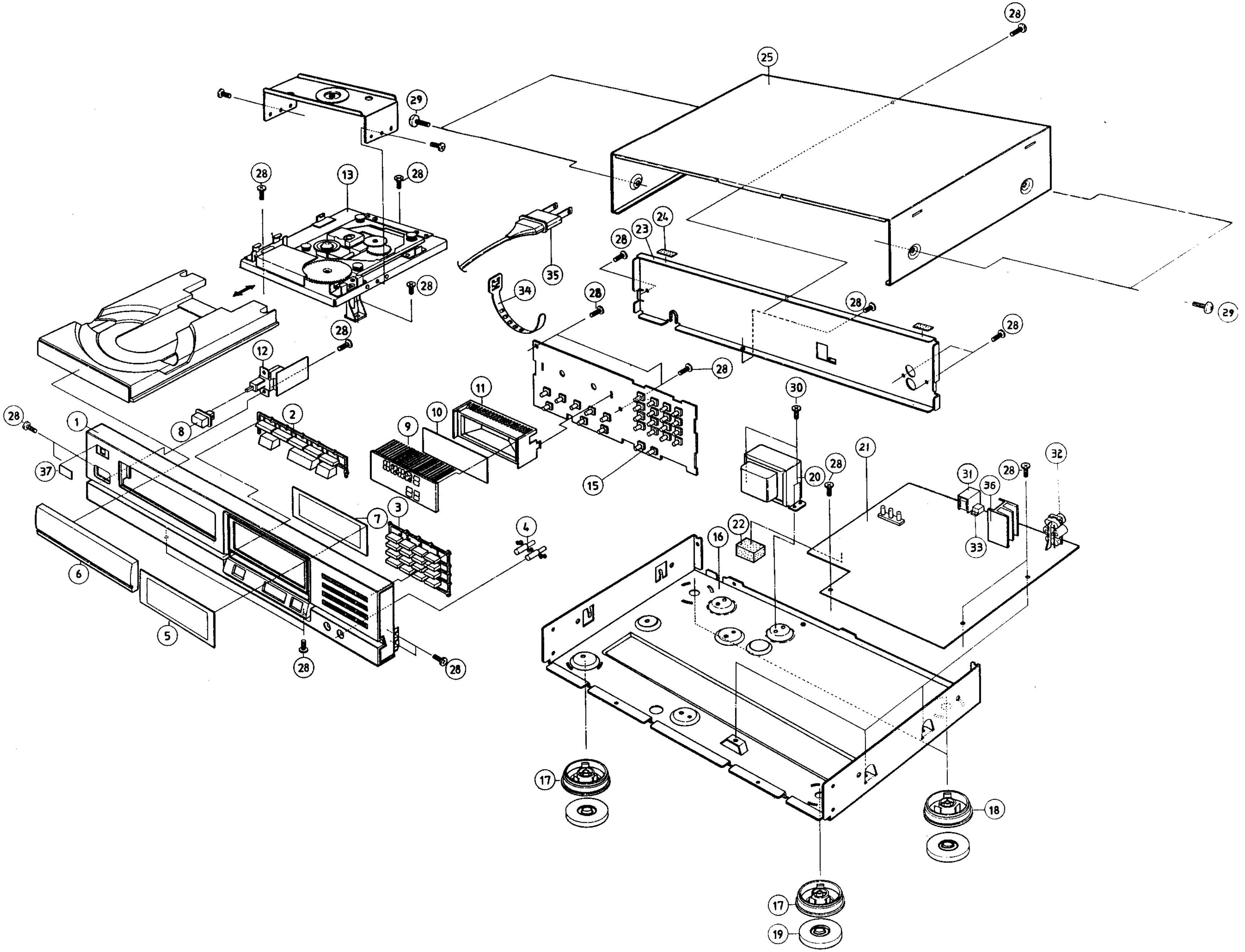
Technische Unterlage

Quelle Technischer Kundendienst 066.3757



BESTELL-NR.	0663757
GERAETEBEZEICHNUNG	UNIV.-CD-PLAYER
WARENGATTUNG	656
AUSFUEHRUNGS-NR.	001
GERAETEBESCHREIBUNG	
PRIVILEG	CD 46011
LIEFERANTEN-NR.	205476
PREIS	499.00
KATALOG	904
GARANTIEZEIT	6
KD-SEKTOR	R
HEIM/BRINGE	WERKSTATT
BETREUUNG	EIGEN
KOSTENTRAEGER	EIGEN
REPARATURFAEHIG	JA

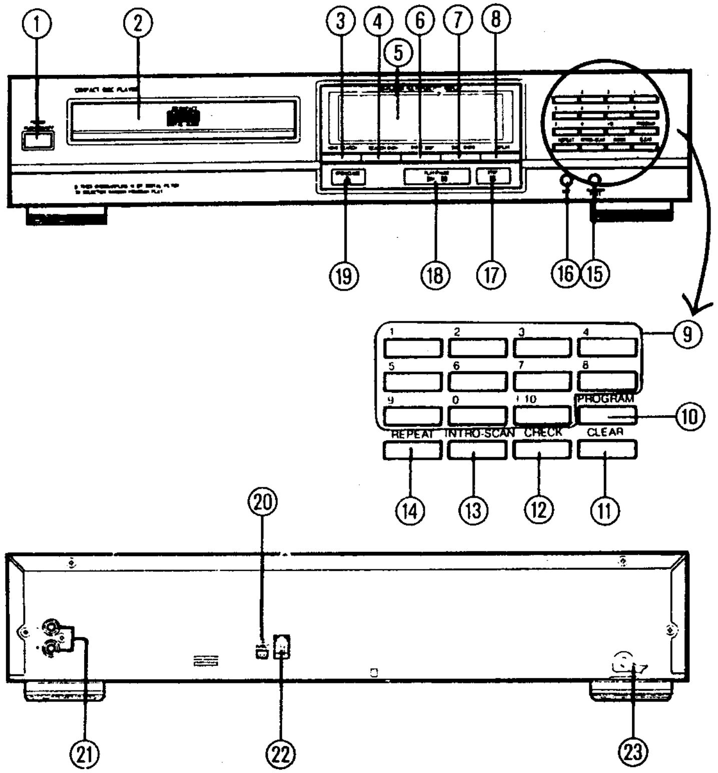


ZEILE	POSITION	SYM BEZEICHNUNG	ET-NUMMER
1			
2		TI 87/90 BEACHTEN :	
3			
4	NF	NF-VERB.KABEL 2X CINCH JE SEITE	997 609 3
5	FB	STEUERKABEL,4-POL	747 036 2
6	FB-SYNCHR.	STEUERKABEL 2-POL	747 037 0
7			
8		GEHAEUSE UND BEDIENTEILE :	
9			
10	1	FRONTBLENDE	747 496 8
11	2	KNOPFLEISTE 8-FACH	747 497 6
12	3	KNOPFPLATTE 16-FACH	747 498 4
13	4	KNOPF,EDIT-RANDOM	747 499 2
14	5	FRONTSCHEIBE	747 501 5
15	6	BLENDE FUER SCHLITTEN	747 495 0
16	7	FILTERSCHEIBE	747 500 7
17	8	KNOPF,POWER	747 035 4
18	12	NETZSCHALTER	741 959 1
19	17	FUSS,VORN	744 824 4
20	18	FUSS,HINTEN	744 825 1
21	19	GUMMIPLATTE FUER FUSS	747 207 9
22	20	NETZTRAFO	747 494 3
23	23	RUECKWAND	747 502 3
24	25	GEHAEUSE-OBERTEIL	747 504 9
25	31	BUCHSE FUER FB 4-POL	746 875 4
26	32	CINCH-BUCHSE	746 769 9
27	33	BUCHSE 2-POL	747 203 8
28	35	ZIERPLATTE AV	747 031 3
29			
30		CD-MECHANIK :	
31			
32		CD-MECHANIK MCD-350	747 273 1
33	9	MOTOR,RF-510T	740 020 3
34	10	MIKROSCHALTER	747 179 0
35	12	KURVENRAD	747 178 2
36	19	CD-SCHLITTEN	747 177 4
37	28	RIEMEN	747 180 8
38			
39		PICK-UP CHASSIS :	
40			
41	2	LASERABTASTEINHEIT KSS-150A	746 735 0
42	9	ZAHNRAD-LASER	747 181 6
43	10	ZAHNRAD-MOTOR	747 182 4
44	13.1,LASER	MOTOR RF-310T-11400 D/V 4,0	743 390 7
45	13.2,DISC	MOTOR RF-310T-11400 D/V 5,9	743 391 5
46	14	MIKROSCHALTER	746 736 8
47			
48		ELEKTRISCHE TEILE :	
49			
50		NETZTRAFO	747 494 3
51		NETZSCHALTER	741 959 1
52		CD-PLATINE	747 490 1
53	AD1-5	DIODE 1 N 4001	176 419 0
54	AIC1,2	IC LM 7805 CT	740 011 2
55	AIC3	IC NJM 4558 S	989 171 4
56	AIC4	IC 7905	954 475 0
57	AL1	SPULE 470 UH	741 989 8
58	LAMP1,2	LAMPE 12V/60MA	747 491 9
59	LCD1	DISPLAY,LCD 8087 MJP	747 222 8
60	TACT-SW	TAST-SCHALTER	747 020 6
61	UD1-7	DIODE 1 N 4148	175 540 4
62	UD9	Z-DIODE RD 5,6 EB1	965 944 2
63	UD14	ZENERDIODE RD 5,1 EB	952 237 6
64	UIC1	IC LC 66508-4528	747 218 6
65	UIC2	IC LC 7582	742 128 2
66	UQ1,3	TRANSISTOR 2 SC 945	175 739 2
67	UQ2	TRANSISTOR 2 SA 733 P	275 032 1
68	UX1	KERAMIK-RESONATOR CSA 4.00 MHZ	741 960 9
69	WIC1	IC CXA 1081 M	742 115 9
70	WIC2	IC CXA 1082 AQ	742 116 7
71	WIC3	IC CXD 1135 Q	742 119 1
72	WIC4	IC CXK 5816-M15L	746 795 4
73	WL1	DROSSEL 10 UH	741 954 2
74	WQ1	TRANSISTOR 2 SB 564 M	924 757 8
75	WQ2,4,6,8	TRANSISTOR KSC 2331 Y	740 016 1
76	WQ3,7,9,11	TRANSISTOR KSA 931 Y	740 014 6
77	WQ5	TRANSISTOR KSR 1003	744 909 3
78	WQ12	TRANSISTOR DTC 124 ES	997 768 7

ZEILE	POSITION	SYM	BEZEICHNUNG	ET-NUMMER
79	XX1		QUARZ, 8.467200 MHZ	732 229 0
80	ZIC1		IC SM 5818 AP	747 492 7
81	ZIC2		IC PCM 61 P	747 493 5
82	ZIC3-5		IC NJM 4558 S	989 171 4
83	ZQ1,3 L-R		TRANSISTOR BD 373 D	951 626 1
			ERSETZT ET-NR. 175 777 2	
84	ZQ2,4		TRANSISTOR KSR 2003	746 866 3

ENDE

BEDIENUNGSELEMENTE



BEDIENUNGSELEMENTE UND FUNKTIONEN

1. **POWER ON/OFF** = EIN/AUS
2. CD-PLATTEN-SCHUBLADE
3. **SEARCH◀◀** = Suchlauf rückwärts
4. **SEARCH▶▶** = Suchlauf vorwärts
5. **Multifunktionsanzeige**
   STOP = Nach dem Beenden der Wiedergabe,
   oder dem Einlegen einer Platte
   PLAY = Wiedergabe-Anzeige
   PAUSE-Anzeige
   REMAIN = Gesamtzeitanzeige der noch verbleibenden
   Spielzeit
   TOTAL = Anzeige der Gesamtspielzeit
   Spielzeitanzeige in Minuten/Sekunden
   REPEAT 1 = Wiederholautomatik eines Titels
   REPEAT ALL = Wiederholautomatik aller Titel
   PROGRAMM-Anzeige
   Kalender-Anzeige; Anzeige der Gesamttitelnummern und der
   noch verbleibenden Titelnummern
6. **SKIP I◀◀** = Titelwahl rückwärts
7. **SKIP▶▶I** = Titelwahl vorwärts
8. **DISPLAY** = Umschaltung der Anzeigeart Spielzeit/Titel.
9. Nummern-Tasten; Zur direkten Titelwahl
10. **PROGRAM** = Speichern der Abspielreihenfolge
11. **CLEAR** = Programmspeicher löschen
12. **CHECK** = Überprüfen der Abspielreihenfolge
13. **INTRO-SCAN** = Kurzes Anspielen aller Titel
14. **REPEAT** = Wiederholung der gesamten Platte der programmierten Titel oder eines Titels.
15. **RANDOM PLAY** = Wiedergabe in zufälliger Reihenfolge
16. **EDIT** = Überspielfunktion
17. **STOP** = Beenden der Wiedergabe
18. **PLAY/PAUSE▶I** = Starten der Wiedergabe und Wiedergabeunterbrechung
19. **OPEN/CLOSE** = zum Öffnen und Schließen des Plattenfaches/Abbrechen der Wiedergabe

Rückseite

20. **CD-IN/OUT** = Synchron-Anschluß für Verstärker V 46012 Best. Nr. 066.369 0 – 066.368 – 066.367
21. **CD-OUTPUT** = Tonleitungsanschluß
22. **SYSTEM CONTROL** = Anschlußbuchse für Fernbedienung
23. Netzanschlußkabel nur 220V [illegible]Herz

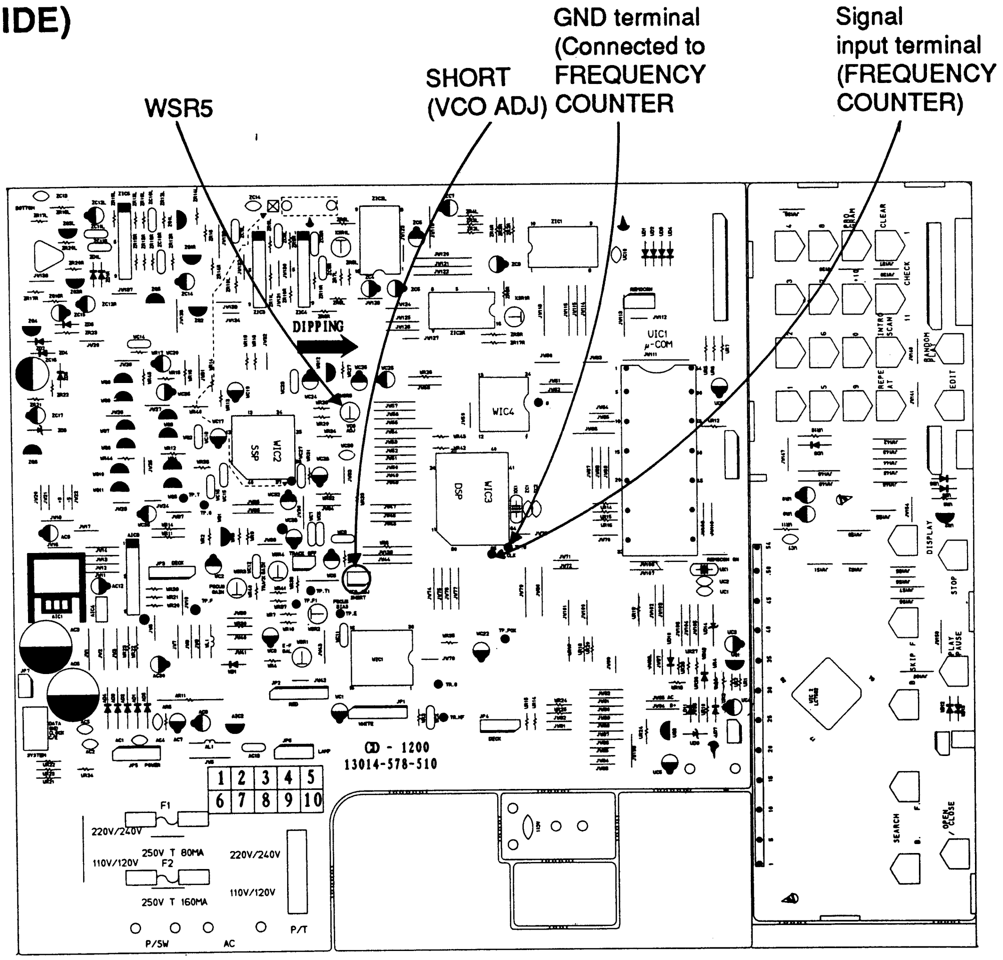
9. ADJUSTMENT

9-1. VCO ADJUSTMENT PRODCEDURE

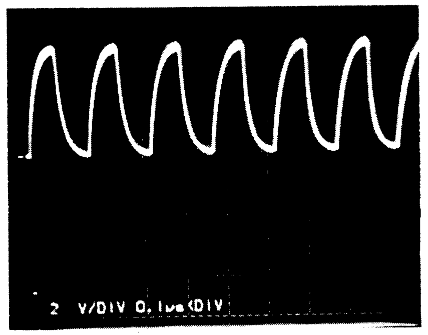
- **10 : 1 damping probe.**

1. Turn power on
2. Close door and adjust while inopertive
3. Connect Frequency Counter GND terminal to TP-G
4. Connect the signal input terminal to TP CLK
5. Short out VCO adjusting port
6. Adjust WSR5 with adjustment jig so that Frequency counter reads 4.321~4.322MHz.

(PARTS SIDE)

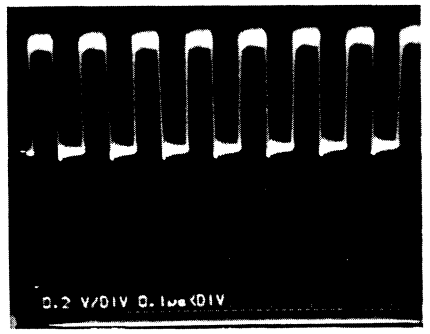

WSR5
SHORT
(VCO ADJ)
GND terminal
(Connected to
FREQUENCY
COUNTER
Signal
input terminal
(FREQUENCY
COUNTER)
DIPPING
CD - 1200
13014-578-510

#13



1:1

#4

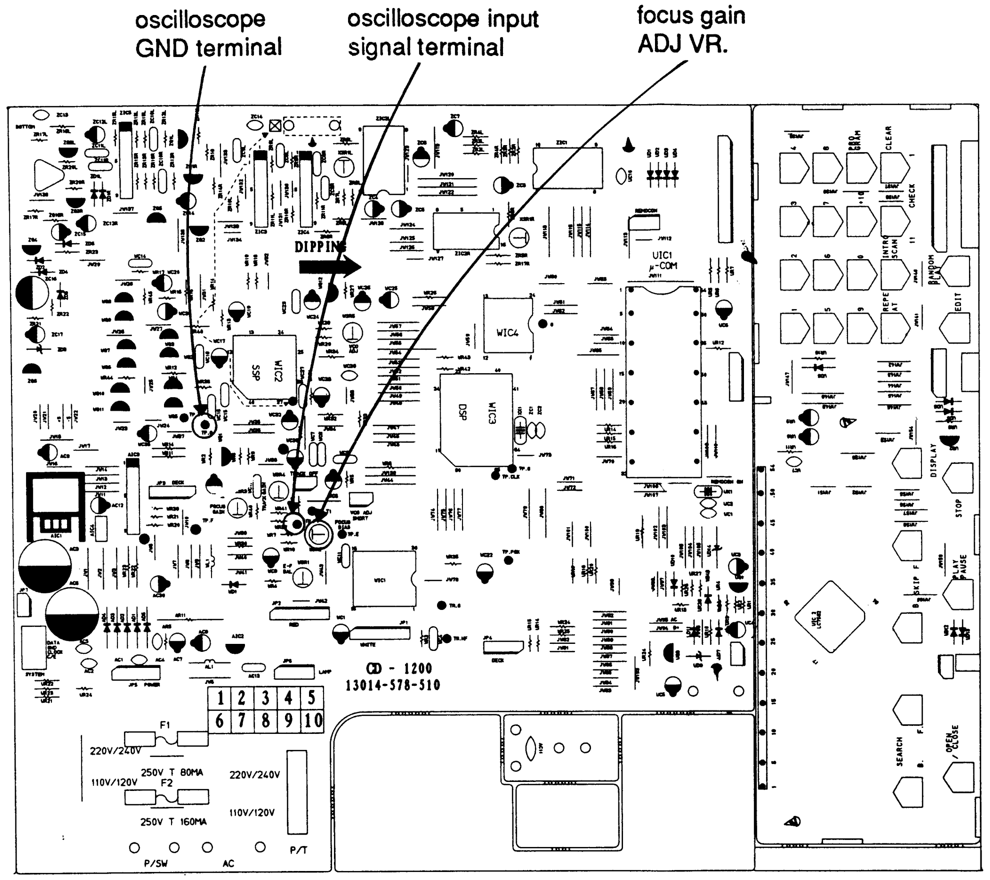


10 : 1

9-2. FOCUS BIAS ADJUSTMENT

1. Adjust while stopped.
2. Connect GND terminal in the Oscilloscope to TP-G.
3. Connect signal input terminal in the oscilloscope to TP-2.
4. Adjust WSR2 so that voltage is 200mV + 0.05V

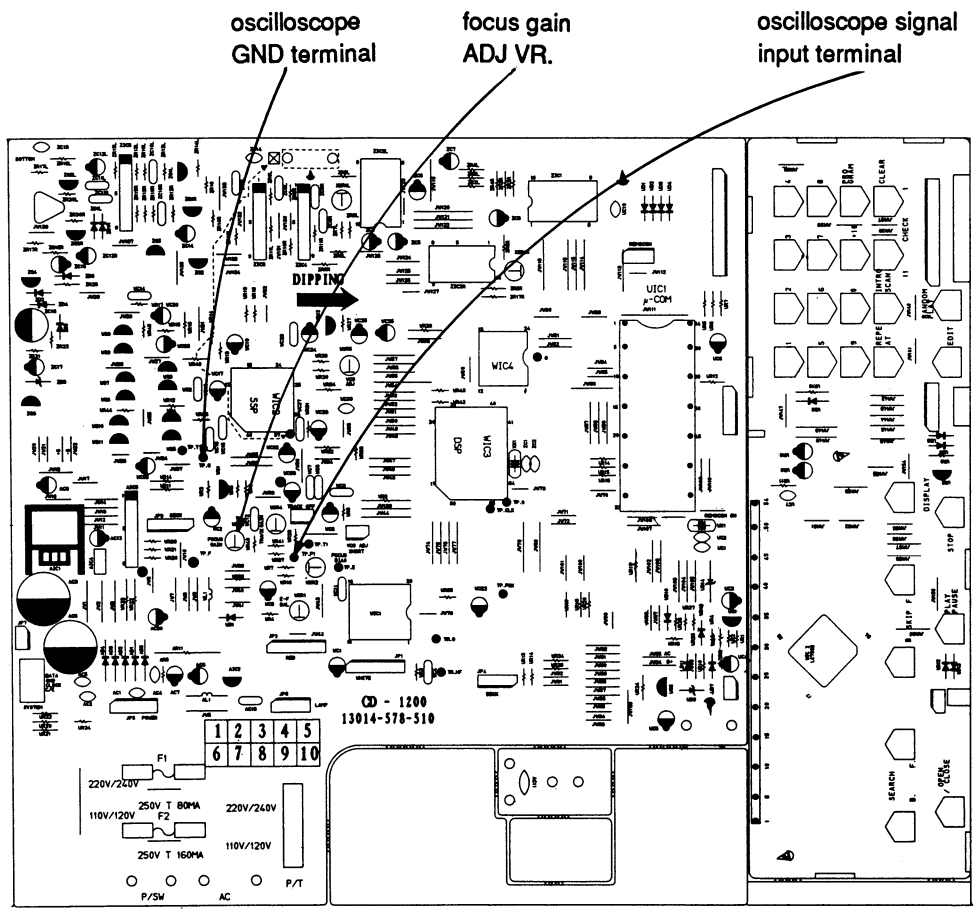
(PARTS SIDE)


oscilloscope
GND terminal
oscilloscope input
signal terminal
focus gain
ADJ VR.
DIPPING
CD - 1200
13014-578-510

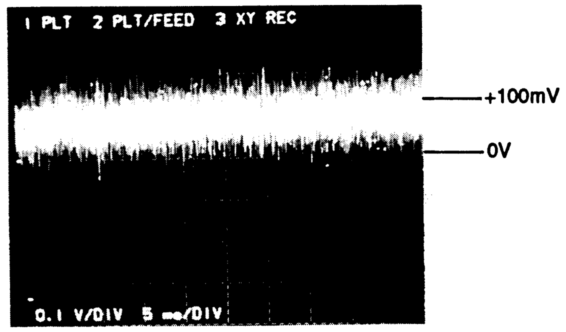
9-3. FOCUS GAIN ADJUSTMENT

1. Adjust during operation.
2. Connect GND terminal on the oscilloscope to TP, G.
3. Connect signal input terminal on the oscilloscope TP. E1.
4. Adjust WSR2 so that the center of peak to peak signal becomes DC 100mv on the oscilloscope.

(Parts SIDE)


oscilloscope GND terminal
focus gain ADJ VR.
oscilloscope signal input terminal
DIPPING
UIC1 µ-COM
WIC4
WIC3
DSP
CD - 1200
13014-578-510
1 2 3 4 5
6 7 8 9 10
F1
F2
220V/240V
110V/120V
250V T 80MA
250V T 160MA
P/SW
AC
P/T
CLEAR
CHECK
EDIT
DISPLAY
STOP
PLAY PAUSE
SEARCH
OPEN/CLOSE

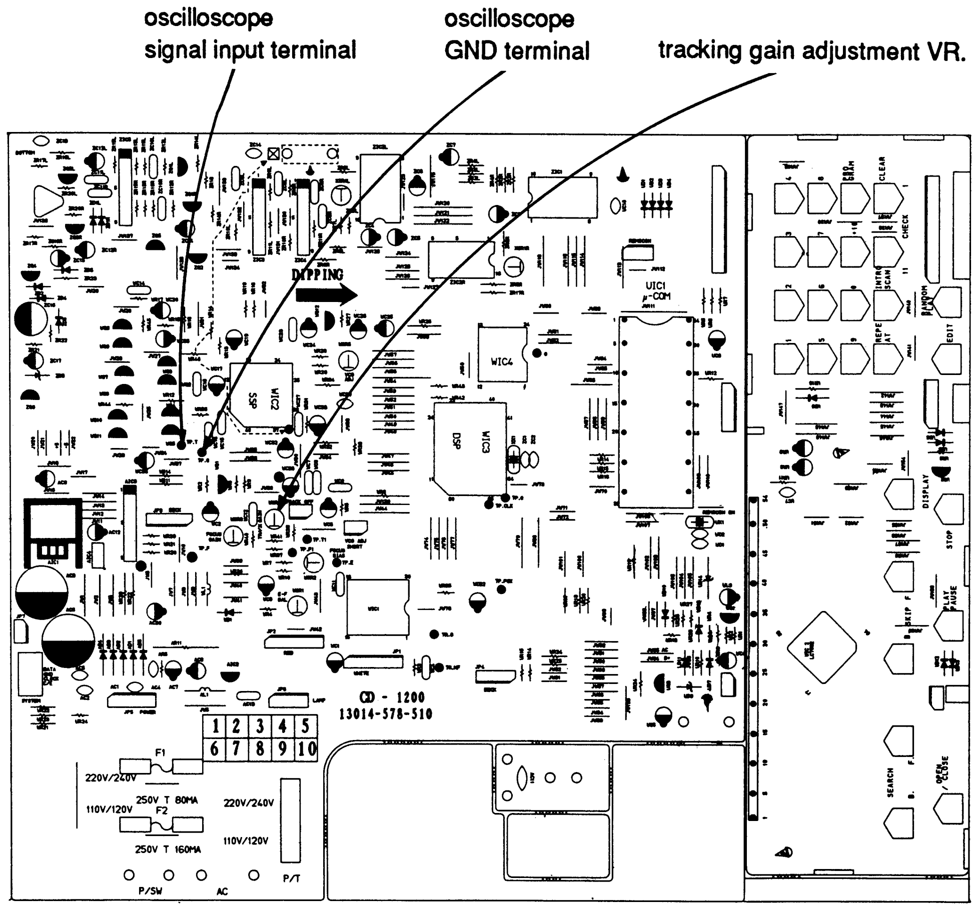
#22



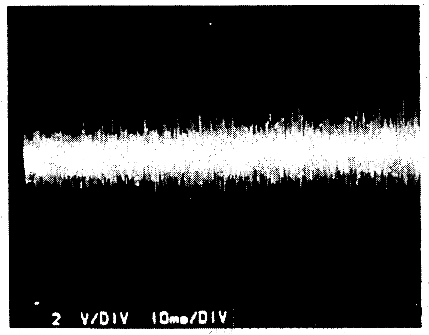
9-4. FOCUS GAIN ADJUSTMENT

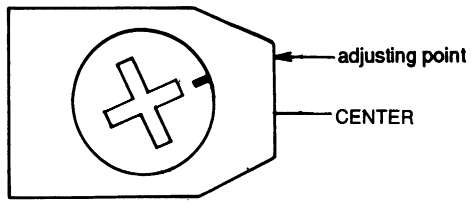
1. Adjust during operation.
2. Connect GND terminal to TP. G.
3. Connect signal input terminal to TP. T.
4. Adjust WSR4 to the position shown in the figure.

(PARTS SIDE)


oscilloscope signal input terminal
oscilloscope GND terminal
tracking gain adjustment VR.
DIPPING
UIC1 µ-COM
WIC4
WIC3
DSP
CD - 1200
13014-578-510
1 2 3 4 5
6 7 8 9 10
F1
F2
220V/240V
110V/120V
250V T 80MA
250V T 160MA
P/SW
AC
P/T
CLEAR
CHECK
EDIT
DISPLAY
STOP
SEARCH

#21



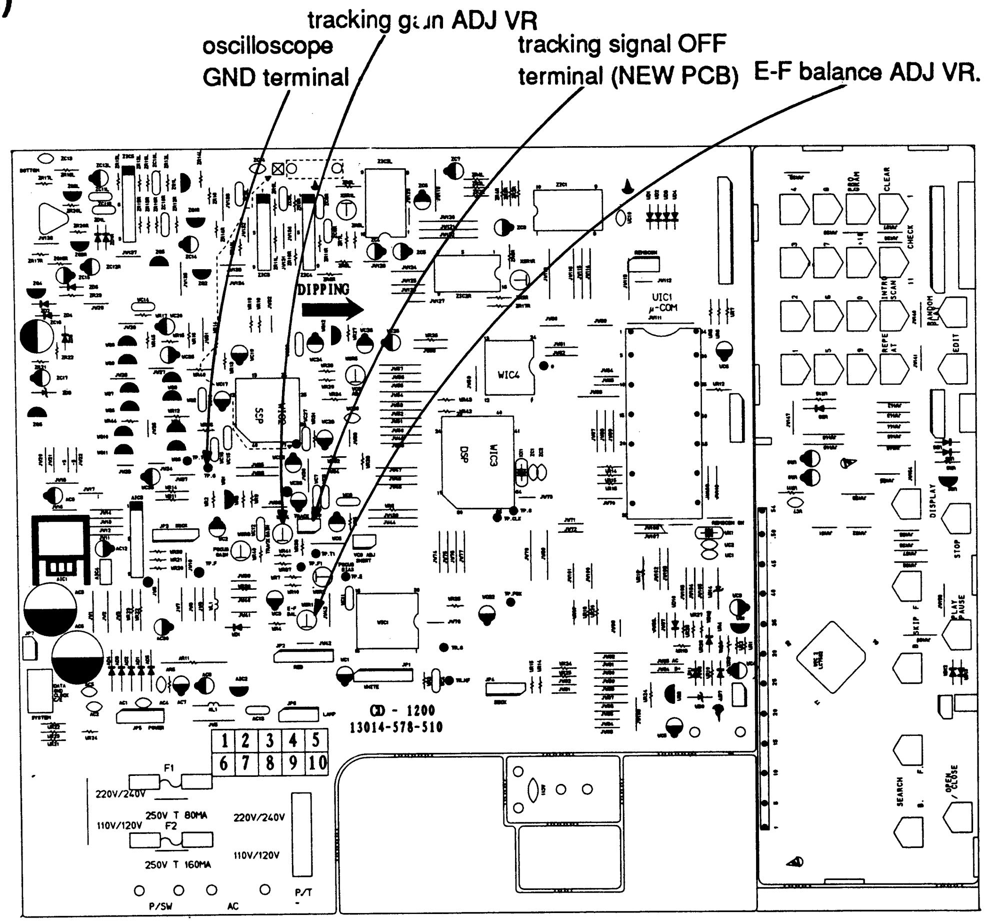

adjusting point
CENTER

WSR4

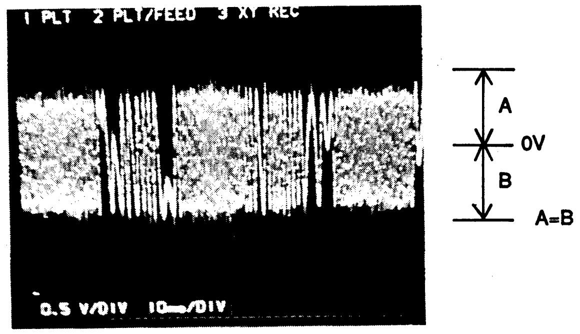
9-5. E-F BALANCE ADJUSTMENT

1. Adjust after playing in mid disc.
2. Set VOLT/DIV of oscilloscope to 0.5mv.
3. Set TIME/DIV of oscilloscope to 10mv.
4. Connect signal input terminal to TP. T1.
5. Connect GND terminal to TPG.
6. Adjust SEMI-VR WSR4 to the counter clockwise direction as much as possible.
7. Adjust WSR1 so that waveform becomes +8mv~-8mv.
8. As for new PCB, adjust by shorting TRACKING SIGNAL.OFF terminal.

(PARTS SIDE)

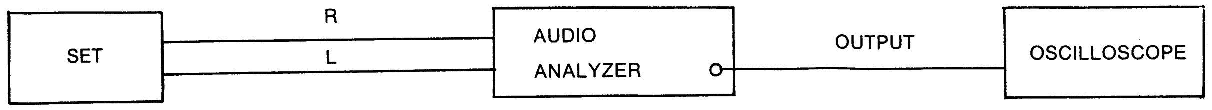

tracking gain ADJ VR
oscilloscope GND terminal
tracking signal OFF terminal (NEW PCB)
E-F balance ADJ VR.
DIPPING
UIC1 μ-COM
UIC4
UIC3
DSP
CD - 1200
13014-578-510
1 2 3 4 5
6 7 8 9 10
F1
F2
220V/240V
110V/120V
250V T 80MA
250V T 160MA
P/SW
AC
P/T

#16

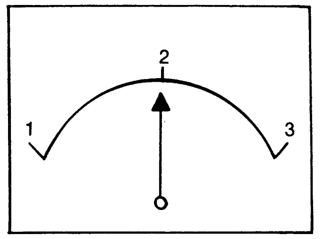


9-6. DAC MSB ADJUSTMENT

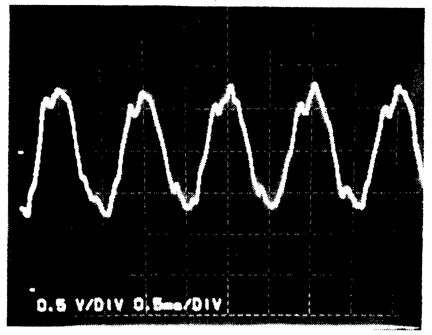
1. Adjust while playing.
2. Play the TEST DISC(1KHz – 60 dB TRACK).
3. Connect RCA output jack to the AUDIO ANALYZER input jack.
4. Set AUDIO ANALYZER function to VOLUME.
5. Connect monitor output of AUDIO ANALYZER to CH1 of oscilloscope .
6. Set the VOLT METER range of AUDIO ANALYZER to 2mv adjusting XSR1 L.R.
7. Adjust XSRIL, R so that the frequency shown in the figure doesnt distort.

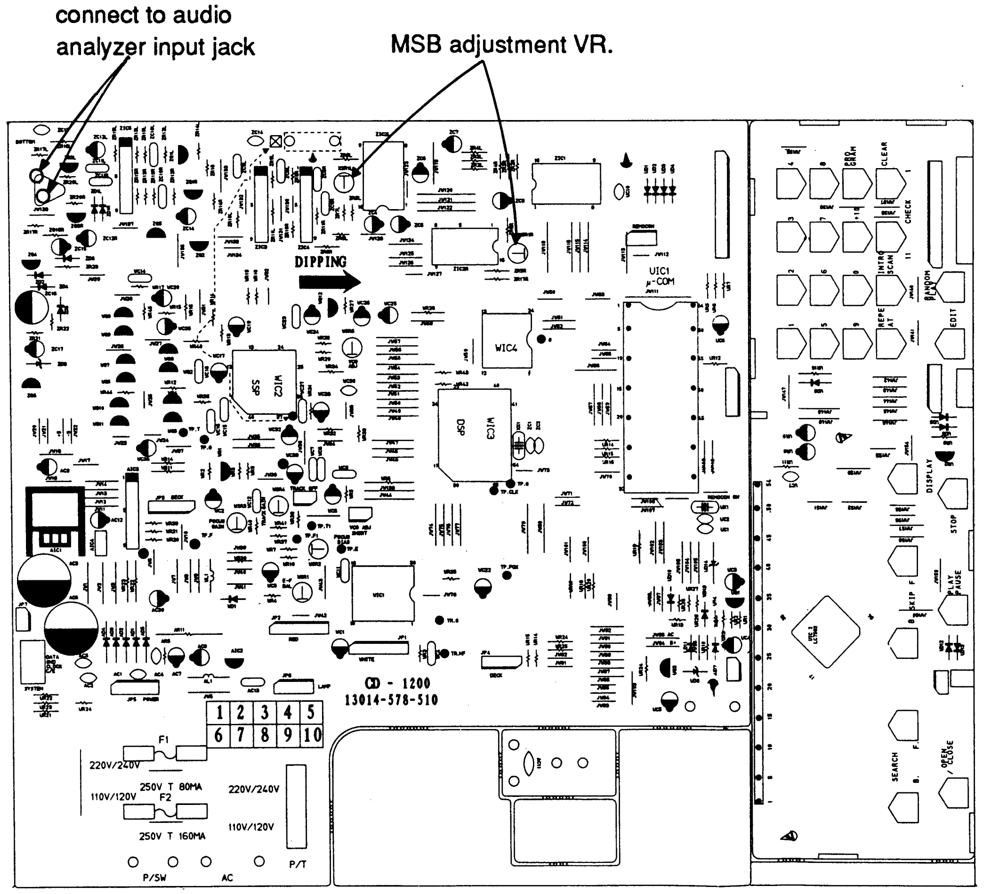

SET
R
L
AUDIO ANALYZER
OUTPUT
OSCILLOSCOPE

1KHz –60dB OUT DISC

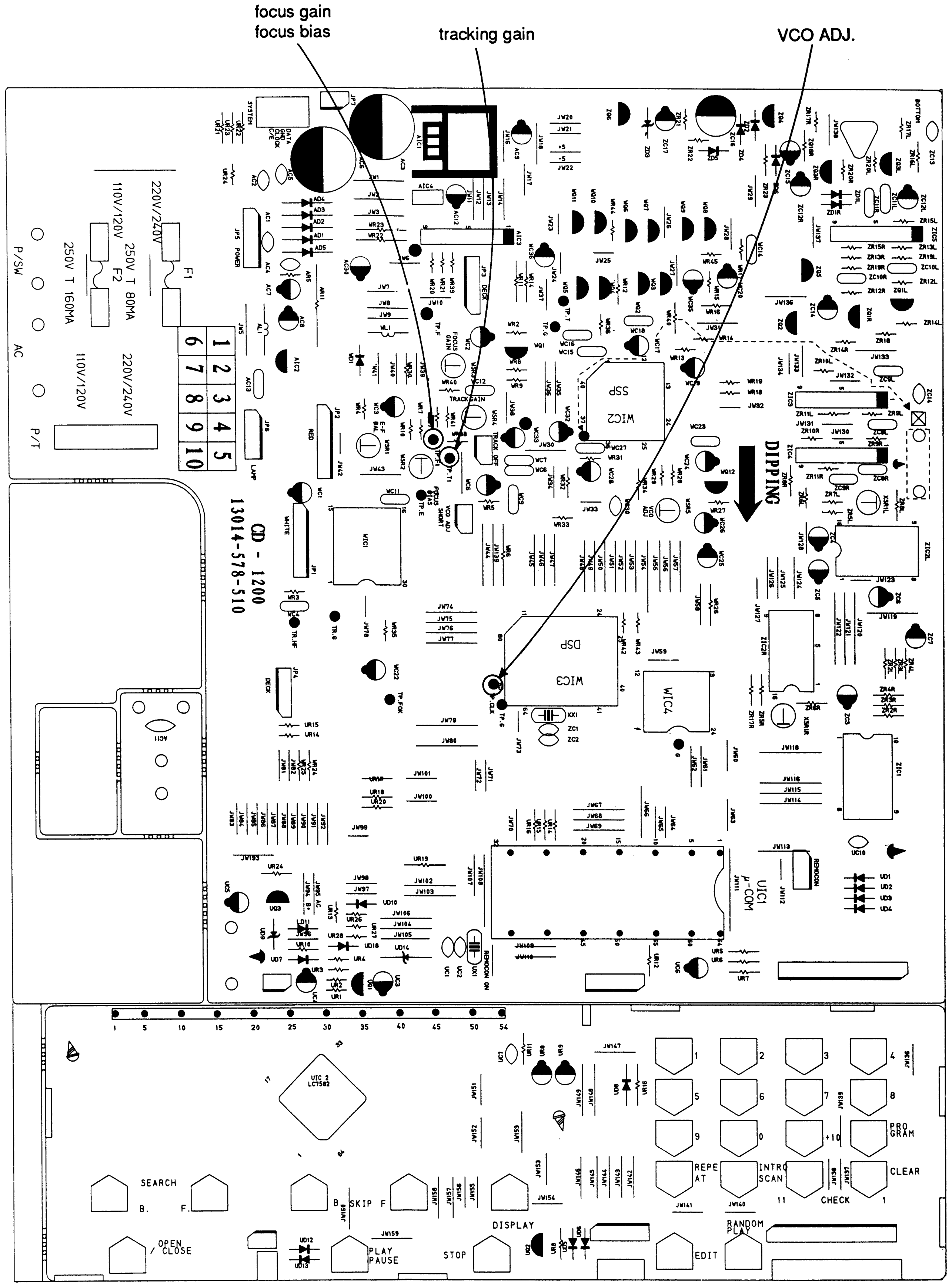


#26

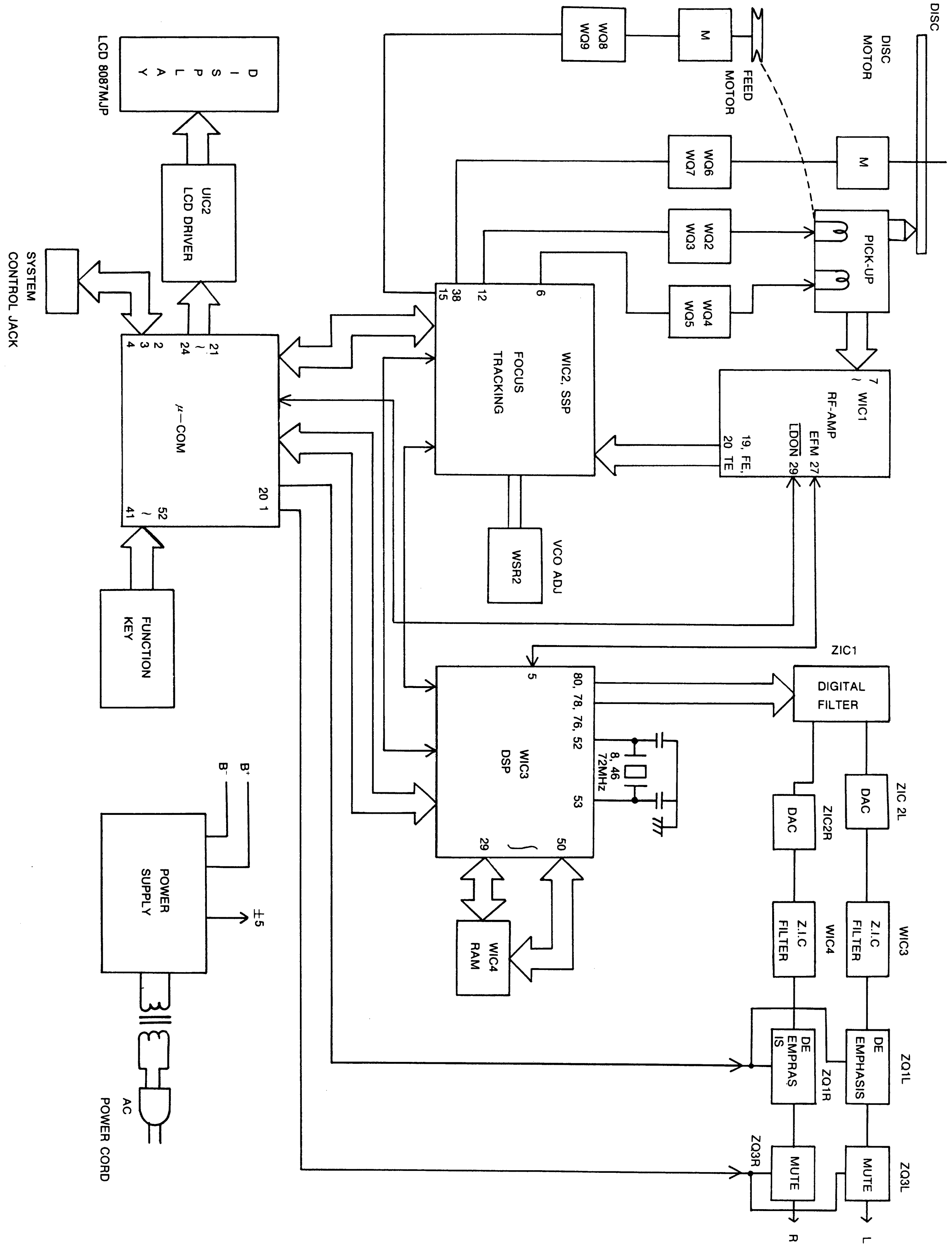



connect to audio analyzer input jack
MSB adjustment VR.
DIPPING
UIC1 μ-COM
UIC4
UIC3
DSP
CD - 1200
13014-578-510
1 2 3 4 5
6 7 8 9 10
F1
F2
220V/240V
110V/120V
250V T 80MA
250V T 160MA
P/SW
AC
P/T

10. ALIGNMENT POINT LOCATION

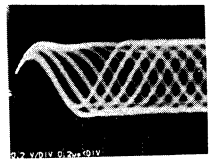

focus gain
focus bias
tracking gain
VCO ADJ.
DIPPING
CD - 1200
13014-578-510
WIC2 SSP
WIC3 DSP
WIC4
UIC1 μ-COM
UIC 2 LC7582
220V/240V
110V/120V
250V T 80MA
250V T 160MA
F1
F2
P/SW
AC
P/T
SEARCH B. F.
B SKIP F
OPEN / CLOSE
PLAY PAUSE
STOP
DISPLAY
EDIT
RANDOM PLAY
REPEAT
INTRO SCAN
CHECK
CLEAR
PROGRAM

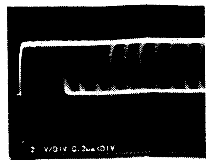
11. BLOCK DIAGRAM

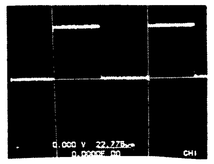

DISC
DISC MOTOR
FEED MOTOR
M
WQ8 WQ9
WQ6 WQ7
WQ2 WQ3
WQ4 WQ5
PICK-UP
WIC1 RF-AMP
7 ~ EFM 27
LDON 29
19, FE,
20 TE
WIC2, SSP
FOCUS
TRACKING
38
15
12
6
VCO ADJ
WSR2
μ-COM
21 ~ 24
2
3
4
20 1
52 ~ 41
FUNCTION KEY
SYSTEM CONTROL JACK
UIC2 LCD DRIVER
DISPLAY
LCD 8087MJP
WIC3 DSP
80, 78, 76, 52
5
53
29
50
8.46 72MHz
WIC4 RAM
ZIC1
DIGITAL FILTER
DAC
ZIC 2L
ZIC2R
Z.I.C FILTER
WIC3
WIC4
DE EMPHASIS
ZQ1L
DE EMPRAS IS
ZQ1R
MUTE
ZQ3L
ZQ3R
L
R
POWER SUPPLY
B+
B-
±5
AC POWER CORD

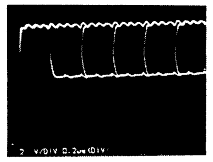
12. SCHEMATIC DIAGRAM AND IC, TR VOLTAGE READING

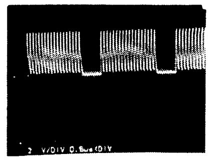
12-1. SCHEMATIC DIAGRAM

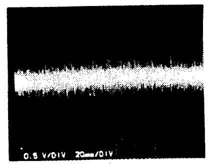

- TP, RF

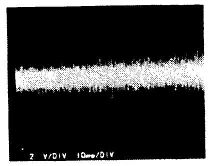

- EFMI

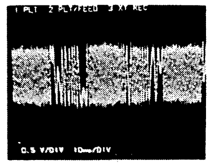

- LRCI


- DIN


- BCKO

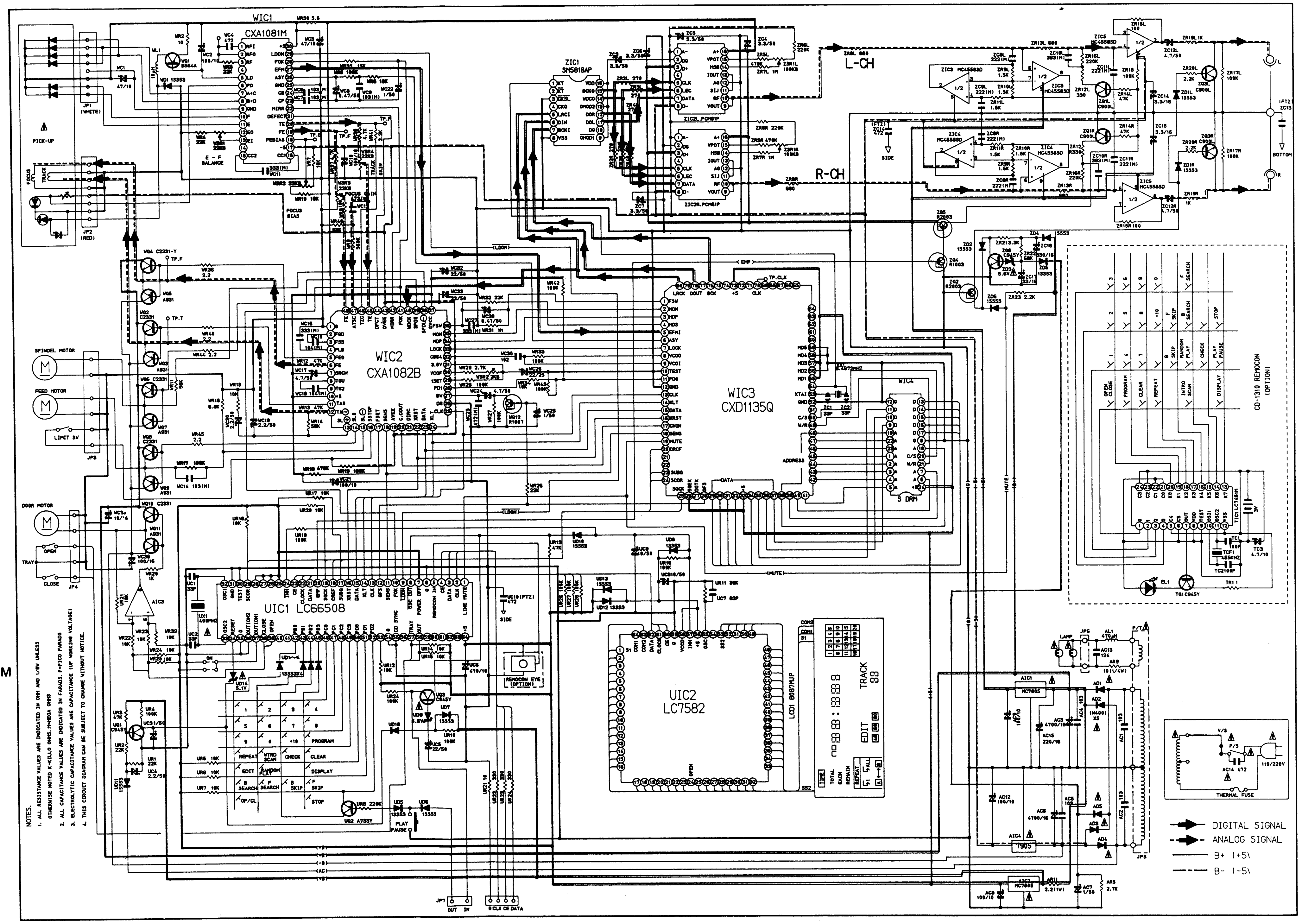

- **FOCUS**


- **TRACKING**


- **WIC1 PIN 19**

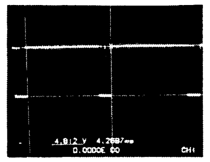
E-F BALANCE

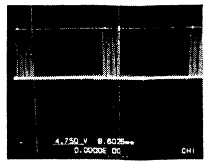
* THIS SCHEMATIC DIAGRAM MAY BE CHANGED FOR IMPROVEMENT WITHOUT ADVANCE NOTED.

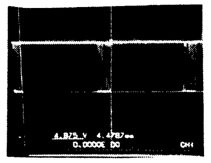

WIC1 CXA1081M
WIC2 CXA1082B
WIC3 CXD1135Q
WIC4
ZIC1 SM5818AP
ZIC2L PCM61P
ZIC2R PCM61P
ZIC3 MC4558SD
ZIC4 MC4558SD
ZIC5 MC4558SD
L-CH
R-CH
UIC1 LC66508
UIC2 LC7582
LCD1 6087MJP
PICK-UP
JP1 (WHITE)
JP2 (RED)
SPINDEL MOTOR
FEED MOTOR
LIMIT SW
DOOR MOTOR
TRAY
OPEN
CLOSE
JP4
FOCUS BIAS
E-F BALANCE
TRACK
EDIT
GD-1310 REMOCON (OPTION)
REMOCON EYE (OPTION)
PLAY PAUSE
OUT IN
THERMAL FUSE
110/220V
DIGITAL SIGNAL
ANALOG SIGNAL
B+ (+5)
B- (-5)

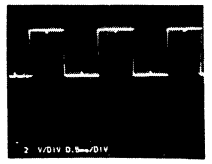
NOTES.

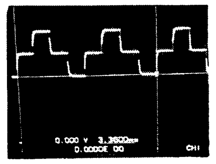
1. ALL RESISTANCE VALUES ARE INDICATED IN OHM AND 1/8W UNLESS OTHERWISE NOTED K=KILLO OHMS, M=MEGA OHMS
2. ALL CAPACITANCE VALUES ARE INDICATED IN FARADS. P=PICO FARADS
3. ELECTROLYTIC CAPACITANCE VALUES ARE CAPACITANCE (UF WORKING VOLTAGE)
4. THIS CIRCUIT DIAGRAM CAN BE SUBJECT TO CHANGE WITHOUT NOTICE.


UIC1 DATA


UIC1 CLOCK


UIC1 CLK


UIC2. S1~S52


UIC2 COM1, 2

12-2. TR, IC VOLTAGE READING

COM (UCI 1)

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
VOLT	5^{4}	5	5	5	0	0	5	5, 4	5	4	$0.^{3}$	0	4, 7	4, 8	4,2	5	0	0.4	5	0	4.3	0.2
PIN	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
VOLT	/	4.3	5	5	5	5	0	0	0	2	2.3	5.5	0	0	0	0	0	4.9	4.9	4.9	4.9	4.9
PIN	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64		
VOLT	4.9	4.9	4.9	4.9	4.9	5	5	5	5	0	0	5	0	5	5	5	5	5	5	5		

1135 (WIC 3)

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
VOLT	0	0	0	0	$2.^{3}$	$2.^{5}$	0	$2.^{4}$	$2.^{3}$	0	$3.^{2}$	0	$4.^{7}$	$4.^{8}$	$4.^{3}$	$4.^{9}$	0	$4.^{5}$	$5.^{5}$	$0.^{4}$	$1.^{3}$	$4.^{5}$
PIN	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
VOLT	0	0	5	5	$2.^{5}$	0	$2.^{6}$	$2.^{7}$	$2.^{6}$	$2.^{2}$	5	$2.^{3}$	$0.^{9}$	4	$2.^{3}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$
PIN	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66
VOLT	$2.^{5}$	0	0	0	0	0	$2.^{5}$	0	$2.^{3}$	$2.^{4}$	5	0	5	0	0	$1.^{3}$	$1.^{3}$	0	$3.^{7}$	$1.^{9}$	$1.^{9}$	$1.^{9}$
PIN	67	68	69	70	71	72	73	74	75	76	77	78	79	80								
VOLT	5	$2.^{5}$	$2.^{5}$	$2.^{4}$	$4.^{9}$	5	5	5	$2.^{5}$	$2.^{5}$	$2.^{5}$	0	$2.^{5}$	$2.^{5}$								

	WQ8	WQ9	WQ7	WQ6	WQ10	WQ11	WQ3	WQ2	WQ4	WQ5
E	0	0	0	0	0	0	0	0	−0.3	0.3
C	$12.^{6}$	−13	−13	$12.^{6}$	$12.^{6}$	−13	−13	$12.^{6}$	$12.^{6}$	−13
B	0.6	0.6	−0.5	−0.5	−0.5	−0.5	0.5	0.5	−0.6	−0.6

ZQ 5			ZQ 4			UQ 3			UQ 1		
E	C	B	E	B	C	E	B	C	E	B	C
5	−4.9	4.9	0	5	14m	$5.^{3}$	$5.^{9}$	$5.^{4}$	0	$-4.^{2}$	$9.^{1}$

ZIC 1 SM5818

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VOLT	$2.^{3}$	$2.^{7}$	0	$2.^{3}$	$2.^{5}$	0	$2.^{5}$	0	5	$2.^{5}$	0	0	5	$2.^{5}$	$1.^{6}$	5

AIC 2 MC7805

IN	G	OUT
$11.^{3}$	0	5

ZIC2L (PCM 61)

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VOLT	−5	0	5	0	$1.^{7}$	$2.^{5}$	0	−5	0	0	0	0	0	$-2.^{5}$	$2.^{5}$	5

AIC 4 MC7905

IN	G	OUT
−13	0	−5

ZQ 6			ZQ 2			WQ 1			ZQ 3L			ZQ 3R			ZQ 1L			ZQ 1R		
E	B	C	E	C	B	E	B	C	E	B	C	E	B	C	E	B	C	E	B	C
0	0.6	6/2	$4.^{7}$	$4.^{7}$	0	5	$4.^{6}$	$0.^{8}$	0	$0.^{7}$	0	0	$0.^{7}$	0	0	$-4.^{9}$	0	0	$-4.^{9}$	0

ZIC2R (PCM 61)

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
VOLT	−5	0	5	0	$1.^{7}$	$2.^{5}$	0	−5	0	0	0	0	0	$-2.^{5}$	$2.^{5}$	5

AIC 1 MC7805

IN	G	OUT
$12.^{7}$	0	5

1081 (UIC 1)

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
VOLT	$-7.^{5}$m	0	$2.^{4}$	0	$4.^{5}$	0	0	0	0	0	0	0	0	−58m	−1
PIN	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
VOLT	$1.^{2}$	−5	$0.^{4}$	$0.^{5}$	0	$-4.^{2}$	0	$-3.^{5}$	0	0	$2.^{5}$	0	$0.^{2}$	$4.^{9}$	5

MC4558S

AIC3	1	2	3	4	5	6	7	8	9	PIN
	$12.^{7}$	$12.^{2}$	0	0	−13	16m	17m	$-0,^{4}$	$12,^{7}$	VOLT
WIC4	5	0	0	0	−5	0	0	0	5	VOLT
WIC3	5	0	0	0	−5	0	0	0	5	VOLT
ZIC5	5	0	0	0	−5	0	0	0	5	VOLT

RAM

PIN	1	2	3	4	5	6	7	8	9	10	11	12
VOLT	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{5}$	$2.^{4}$	4	$0.^{9}$	$0.^{1}$
PIN	13	14	15	16	17	18	19	20	21	22	23	24
VOLT	$2.^{5}$	$2.^{2}$	$2.^{5}$	0	0	0	0	0	0	0	0	5

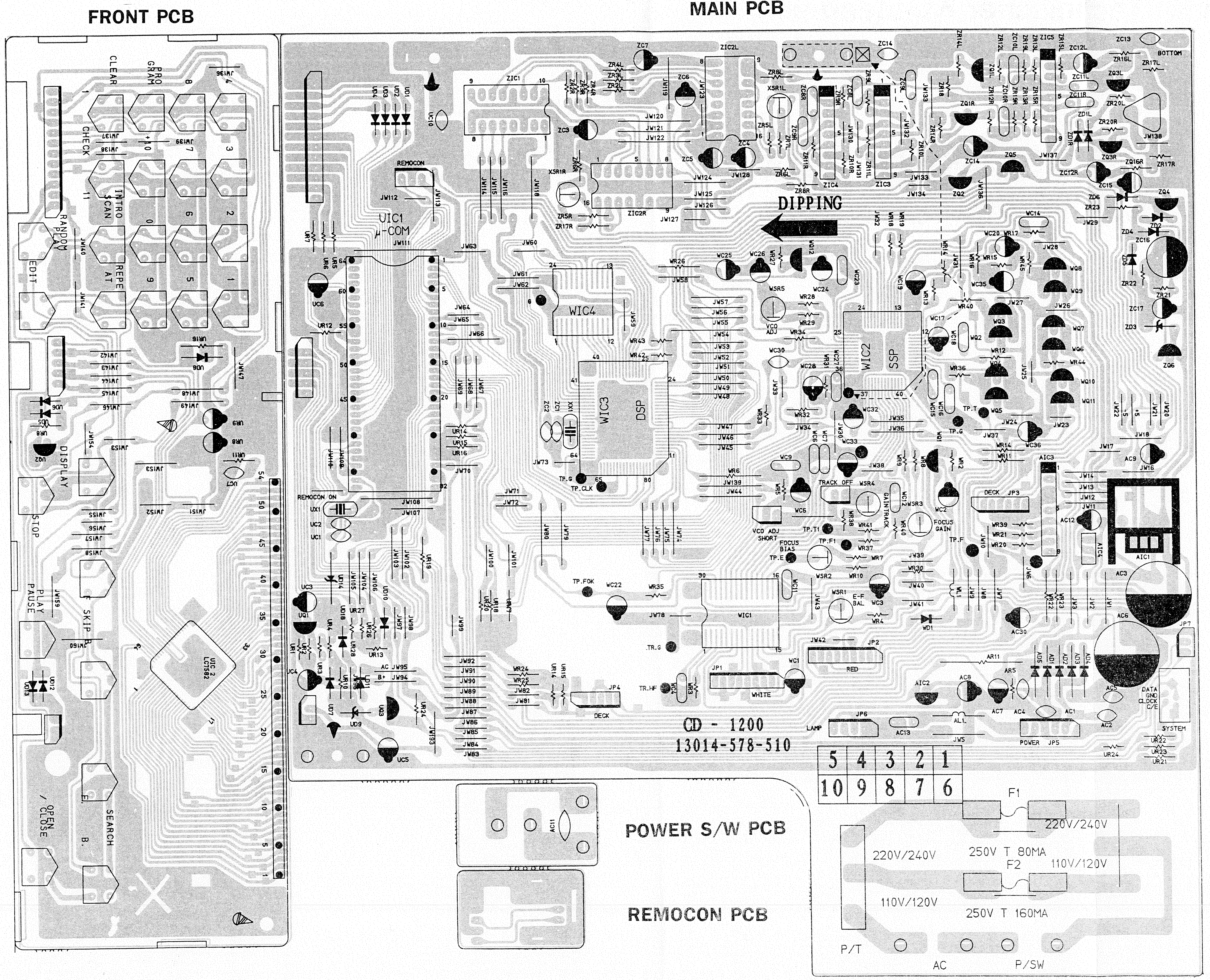
1082 (UIC 2)

PIN	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
VOLT	0	0	0	0	−0.6	0	0.6	0	0	5	0.5	0	0	0.6	0	0	−4	0.3	−5	$0,^{1}$	5	5
VOLT	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
VOLT	4.3	4.8	$4.^{7}$	0	3.2	$3.^{2}$	$2.^{2}$	$2.^{3}$	$3.^{5}$	2	$0.^{2}$	$0.^{2}$	$0.^{2}$	$0.^{2}$	5	0	$-0.^{5}$	$2.^{5}$	$3.^{8}$	0	−5	$-4.^{2}$
PIN	45	46	47	48																		
VOLT	0	0	0	$0,^{6}$																		

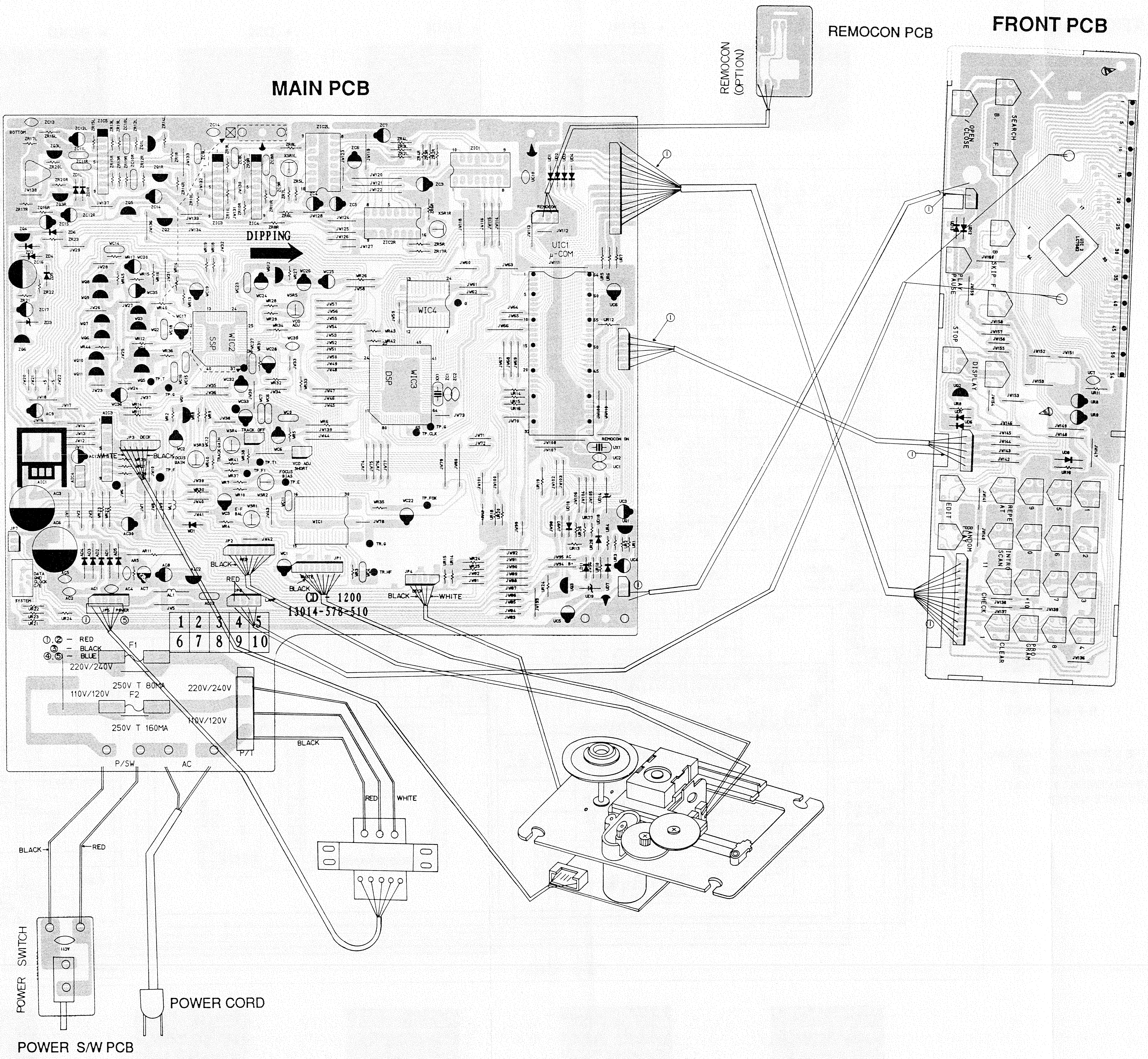
UIC 2 LC7582

PIN	1	2	3	4	5	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	2
VOLT	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$
PIN	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
VOLT	$2.^{2}$	$4.^{4}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$
PIN	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64		
VOLT	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$2.^{2}$	$3.^{7}$	$4.^{4}$	$4.^{4}$	$4.^{4}$	0	1	$0.^{2}$	$4.^{3}$	$2.^{2}$	$2.^{2}$		

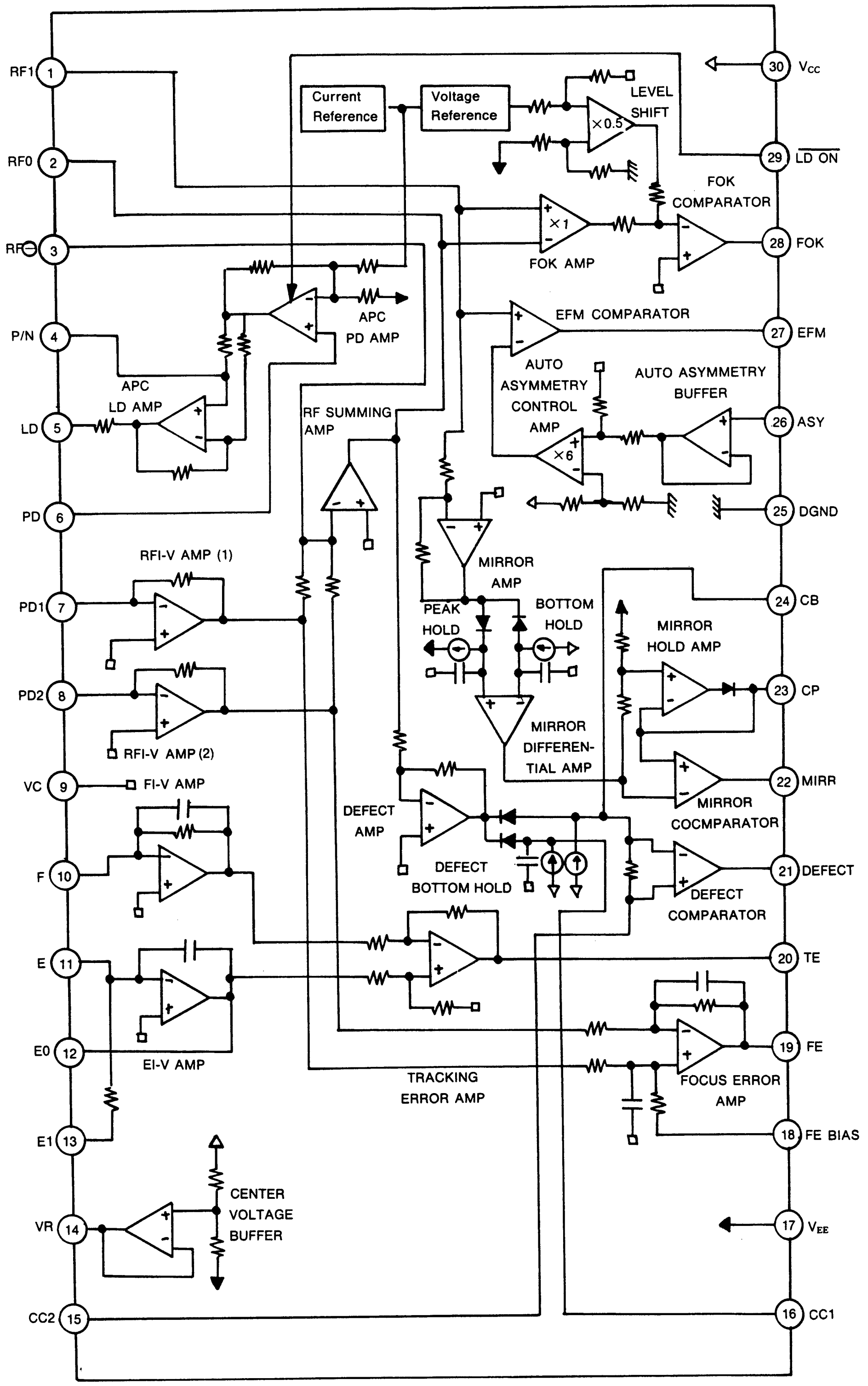
13-2. PATTERN SIDE


FRONT PCB
MAIN PCB
CLEAR
PRO GRAM
CHECK
INTRO SCAN
RANDOM PLAY
EDIT
REPE AT
DISPLAY
STOP
PLAY PAUSE
SKIP
SEARCH
OPEN / CLOSE
UIC 2 LC7582
UIC1 μ-COM
REMOCON
REMOCON ON
ZIC1
ZIC2L
ZIC2R
ZIC3
ZIC4
WIC4
WIC3 DSP
WIC2 SSP
WIC1
AIC1
AIC2
AIC3
DIPPING
VCO ADJ
VCO ADJ SHORT
FOCUS BIAS
FOCUS GAIN
TRACK OFF
GAIN TRACK
E-F BAL
TP.FOK
TP.G
TP.CLK
TP.T
TP.F
TP.E
TR.G
TR.HF
DECK
WHITE
RED
LAMP
POWER JP5
SYSTEM
DATA
GND
CLOCK
C/E
BOTTOM
CD - 1200
13014-578-510
5 4 3 2 1
10 9 8 7 6
F1
F2
220V/240V
110V/120V
250V T 80MA
250V T 160MA
P/T
AC
P/SW
POWER S/W PCB
REMOCON PCB

14. WIRING DIAGRAM


MAIN PCB
REMOCON (OPTION)
REMOCON PCB
FRONT PCB
DIPPING
SSP
WIC2
DSP
WIC3
WIC4
VIC1
μ-COM
BLACK
WHITE
RED
CD 1200
13014-578-510
1 2 3 4 5
6 7 8 9 10
①② - RED
③ - BLACK
④⑤ - BLUE
F1
220V/240V
250V T 80MA
110V/120V
F2
250V T 160MA
220V/240V
110V/120V
P/SW
AC
P/T
BLACK
RED
WHITE
BLACK
RED
OPEN/CLOSE
SEARCH
B.
F.
PLAY PAUSE
SKIP F
STOP
DISPLAY
EDIT
RANDOM PLAY
REPEAT
INTRO SCAN
CHECK
CLEAR
PROGRAM
POWER SWITCH
POWER CORD
POWER S/W PCB

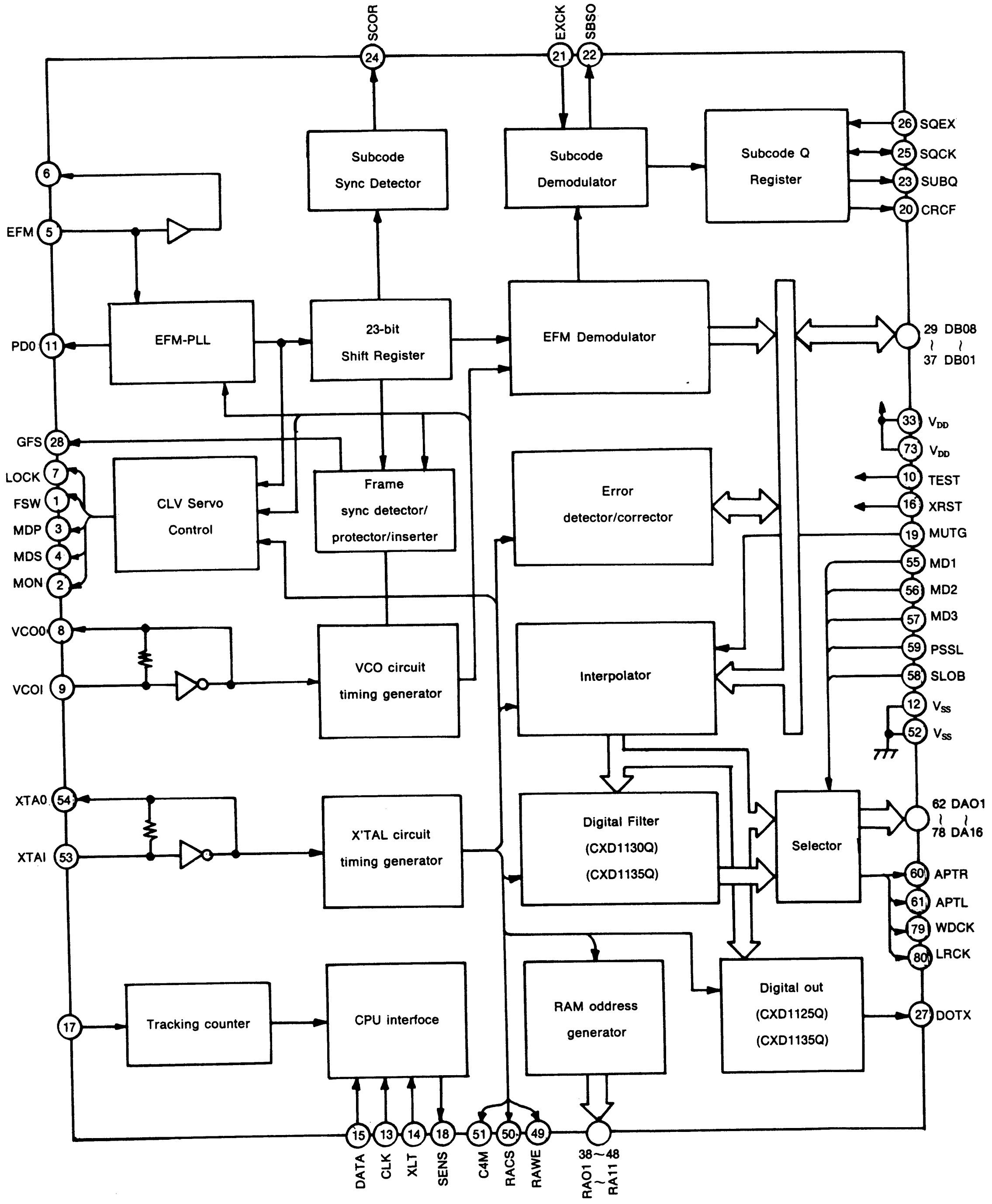
15-3. CXA1081(RF, AMP) : WIC1


RF1 1
RF0 2
RF⊖ 3
P/N 4
LD 5
PD 6
PD1 7
PD2 8
VC 9
F 10
E 11
E0 12
E1 13
VR 14
CC2 15
CC1 16
VEE 17
FE BIAS 18
FE 19
TE 20
DEFECT 21
MIRR 22
CP 23
CB 24
DGND 25
ASY 26
EFM 27
FOK 28
LD ON 29
VCC 30
Current Reference
Voltage Reference
LEVEL SHIFT
×0.5
FOK COMPARATOR
×1
FOK AMP
APC PD AMP
EFM COMPARATOR
AUTO ASYMMETRY CONTROL AMP
×6
AUTO ASYMMETRY BUFFER
APC LD AMP
RF SUMMING AMP
RFI-V AMP (1)
RFI-V AMP (2)
FI-V AMP
MIRROR AMP
PEAK HOLD
BOTTOM HOLD
MIRROR HOLD AMP
MIRROR DIFFEREN-TIAL AMP
MIRROR COCMPARATOR
DEFECT AMP
DEFECT BOTTOM HOLD
DEFECT COMPARATOR
EI-V AMP
TRACKING ERROR AMP
FOCUS ERROR AMP
CENTER VOLTAGE BUFFER

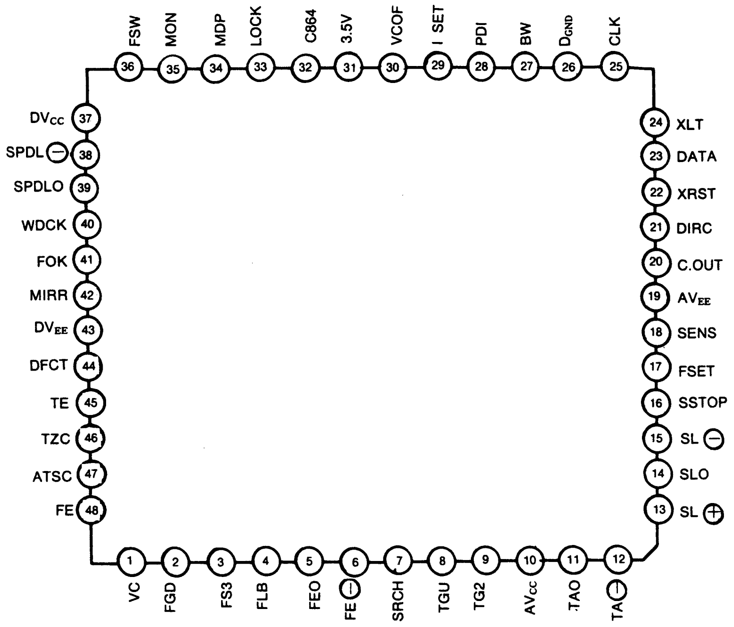
Pin Description (CXD1135Q)

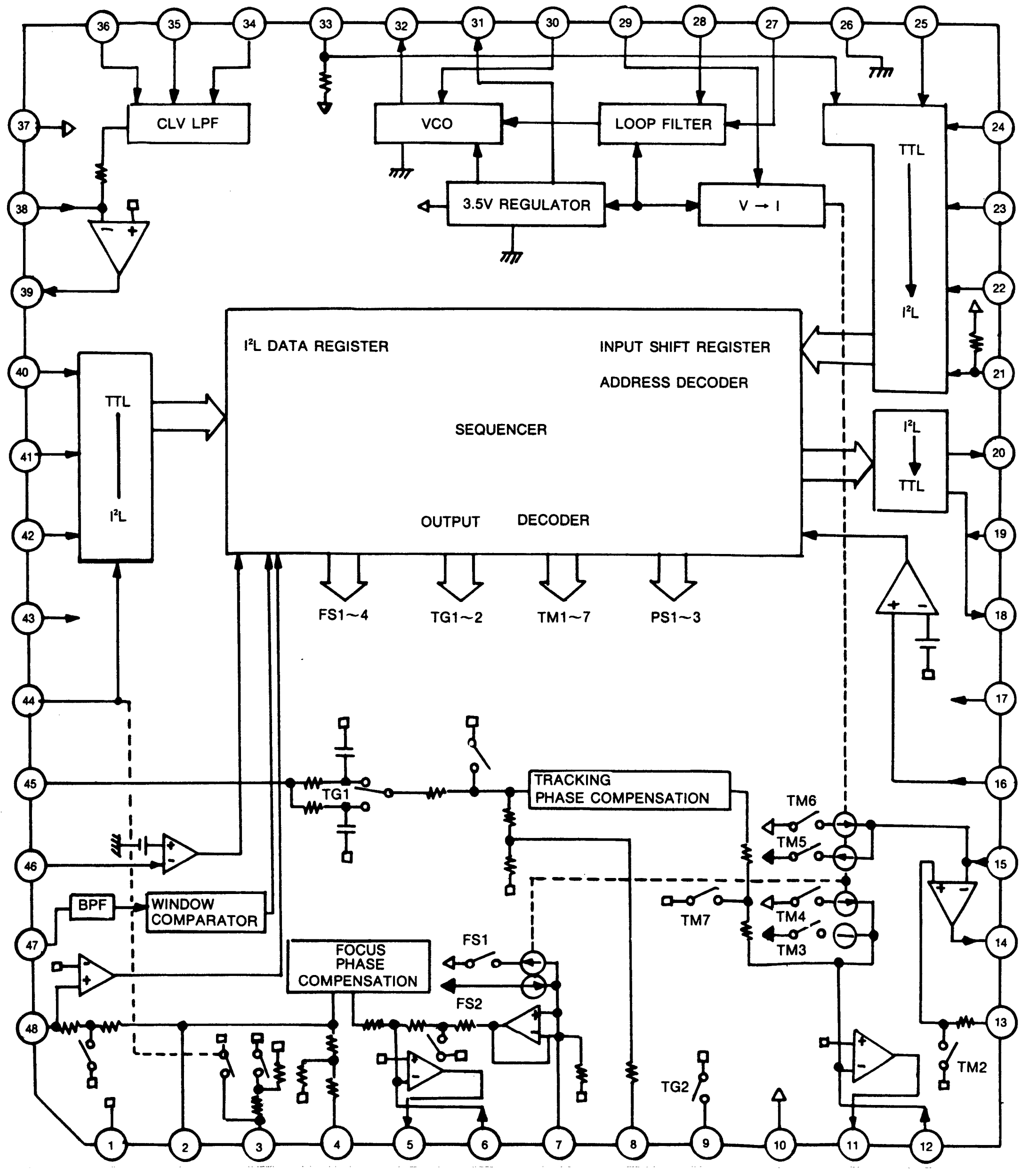
No.	Symbol	I/O	Description
1	FSW	O	Pin 1 output is switched constant when the output filter of the spindle motor is enegized.
2	MON	O	ON/OFF control for spindle motor.
3	MDP	O	Spindle motor drive. Provides rough control during CLV-S mode and phase control during CLV-P mode.
4	MDS	O	Spindle motor drive. Controls speed during CLV-P mode.
5	EFM	I	EFM signal from RF amplifier.
6	ASY	O	Controls slice level of the EFM signal.
7	LOCK	O	The output of pin 7 reflects the status of the GFS signal which is sampled at WFCK/16. When the GFS signal is "H", the output of pin 7 is also "H", but when the signal has remianed "L" for at least 8 samples, the output of pin 7 is "L".
8	VCOO	O	When VCO locks to EFM signal, the frequency becomes 8.6432MHz.
9	VCOI	I	VCO input.
10	TEST	I	(0V)
11	PDO	O	The output of Pin 11 provides phase comparison of EFM signal and VCO/2.
12	Vss	–	GND (0V)
13	CLK	I	Pin 13 provides serial transmission clock from the CPU. Data is latched on the leading edge of the clock.
14	XLT	I	Pin 14 provides latch input from the CPU. 8-bit shift register data (serial data received from the CPU) is latched in each of the registers.
15	DATA	I	Serial data from the CPU.
16	XRST	I	System reset ("L")
17	CNIN	I	Tracking pulse input.
18	SENS	O	Output reflecting internal condition as designated by address.
19	MUTG	I	Muting input. MUTG is "L" when ATTM of internal register A is "L" (normal condition). MUTG is "H" when muting condition is set.
20	CRCF	O	Output the results CRC check of subcode Q.
21	EXCK	I	Clock input for subcode serial output.
22	SBSO	O	Serial output of subcode.
23	SUBQ	O	Output of subode Q.
24	SCOR	O	OUtput of subcode sync S0 + S1.
25	SQCK	I/O	Clock for reading subcode Q.
26	SQEX	I	Input for selecting SQCK.
27	POTX	O	Digital output ($\overline{\text{WFCK}}$ is output when DO is off or for the CXD1130Q)
28	GFS	O	Indicates the frame sync lock status.
29	DB08	I/O	Data pin for exernal RAM. DATA8 (MSB)
30	DB07	I/O	Data pin for external RAM. DATA7
31	DB06	I/O	Data pin for external RAM. DATA6
32	DB05	I/O	Data pin for external RAM. DATA5
33	VDD	–	Power supply (+5V)
34	DB04	I/O	Data pin for external RAM. DATA4
35	DB03	I/O	Data pin for external RAM. DATA3
36	DB02	I/O	Data pin for external RAM. DATA2
37	DB01	I/O	Data pin for external RAM. DATA1 (LSB)
38	RA01	O	Output address of external RAM. ADDR01 (LSB)
39	RA02	O	Output address of external RAM. ADDR02
49	RA03	O	Output address of external RAM. ADDR03

15-4. CXA1135Q(DSP) : WIC3

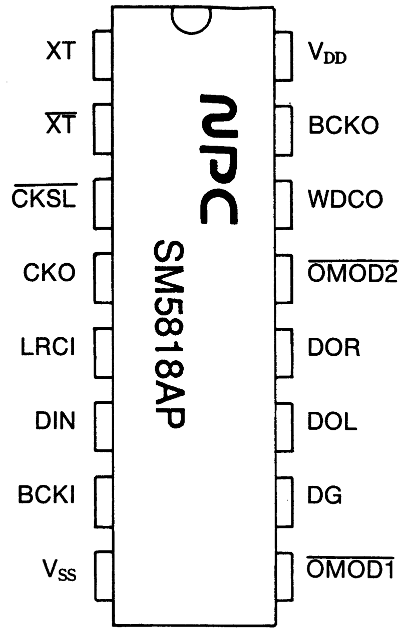

SCOR
EXCK
SBSO
24
21
22
Subcode Sync Detector
Subcode Demodulator
Subcode Q Register
26 SQEX
25 SQCK
23 SUBQ
20 CRCF
6
EFM 5
PDO 11
EFM-PLL
23-bit Shift Register
EFM Demodulator
29 DB08 ~ 37 DB01
33 VDD
73 VDD
10 TEST
16 XRST
19 MUTG
55 MD1
56 MD2
57 MD3
59 PSSL
58 SLOB
12 VSS
52 VSS
GFS 28
LOCK 7
FSW 1
MDP 3
MDS 4
MON 2
CLV Servo Control
Frame sync detector/ protector/inserter
Error detector/corrector
VCOO 8
VCOI 9
VCO circuit timing generator
Interpolator
XTAO 54
XTAI 53
X'TAL circuit timing generator
Digital Filter (CXD1130Q) (CXD1135Q)
Selector
62 DAO1 ~ 78 DA16
60 APTR
61 APTL
79 WDCK
80 LRCK
17
Tracking counter
CPU interfoce
RAM oddress generator
Digital out (CXD1125Q) (CXD1135Q)
27 DOTX
15 DATA
13 CLK
14 XLT
18 SENS
51 C4M
50 RACS
49 RAWE
38~48 RAO1 ~ RA11

15-5. CXA1082AQ(SSP) : WIC2

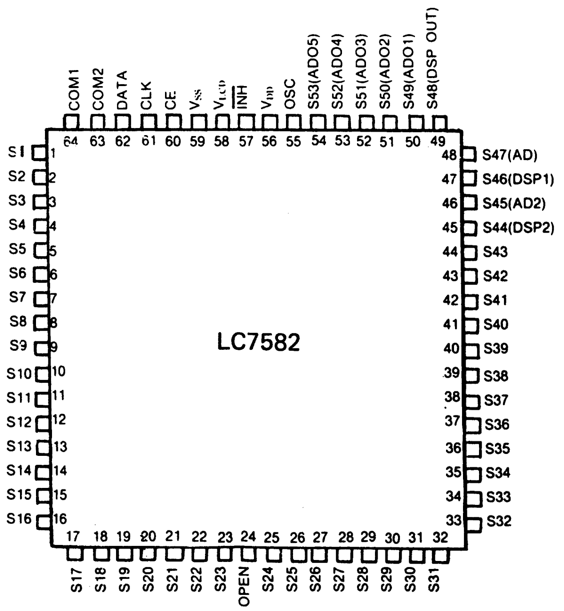

FSW 36
MON 35
MDP 34
LOCK 33
C864 32
3.5V 31
VCOF 30
I SET 29
PDI 28
BW 27
DGND 26
CLK 25
DVCC 37
SPDL⊖ 38
SPDLO 39
WDCK 40
FOK 41
MIRR 42
DVEE 43
DFCT 44
TE 45
TZC 46
ATSC 47
FE 48
24 XLT
23 DATA
22 XRST
21 DIRC
20 C.OUT
19 AVEE
18 SENS
17 FSET
16 SSTOP
15 SL⊖
14 SLO
13 SL⊕
1 VC
2 FGD
3 FS3
4 FLB
5 FEO
6 FE⊖
7 SRCH
8 TGU
9 TG2
10 AVCC
11 TAO
12 TA⊖


36
35
34
33
32
31
30
29
28
27
26
25
CLV LPF
VCO
LOOP FILTER
3.5V REGULATOR
V → I
TTL
I²L
37
38
39
40
41
42
43
44
45
46
47
48
24
23
22
21
20
19
18
17
16
15
14
13
I²L DATA REGISTER
INPUT SHIFT REGISTER
ADDRESS DECODER
SEQUENCER
OUTPUT DECODER
FS1~4
TG1~2
TM1~7
PS1~3
TG1
TRACKING PHASE COMPENSATION
TM6
TM5
TM4
TM7
TM3
BPF
WINDOW COMPARATOR
FOCUS PHASE COMPENSATION
FS1
FS2
TG2
TM2
1
2
3
4
5
6
7
8
9
10
11
12

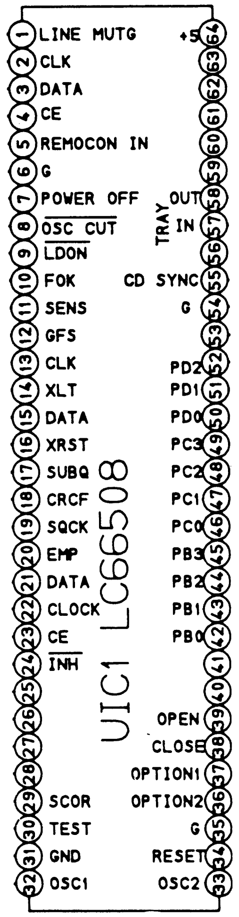
15-6. SM5818AP(DIGITAL FILTER) : ZIC1


XT
XT
CKSL
CKO
LRCI
DIN
BCKI
V_{SS}
V_{DD}
BCKO
WDCO
OMOD2
DOR
DOL
DG
OMOD1
NPC
SM5818AP

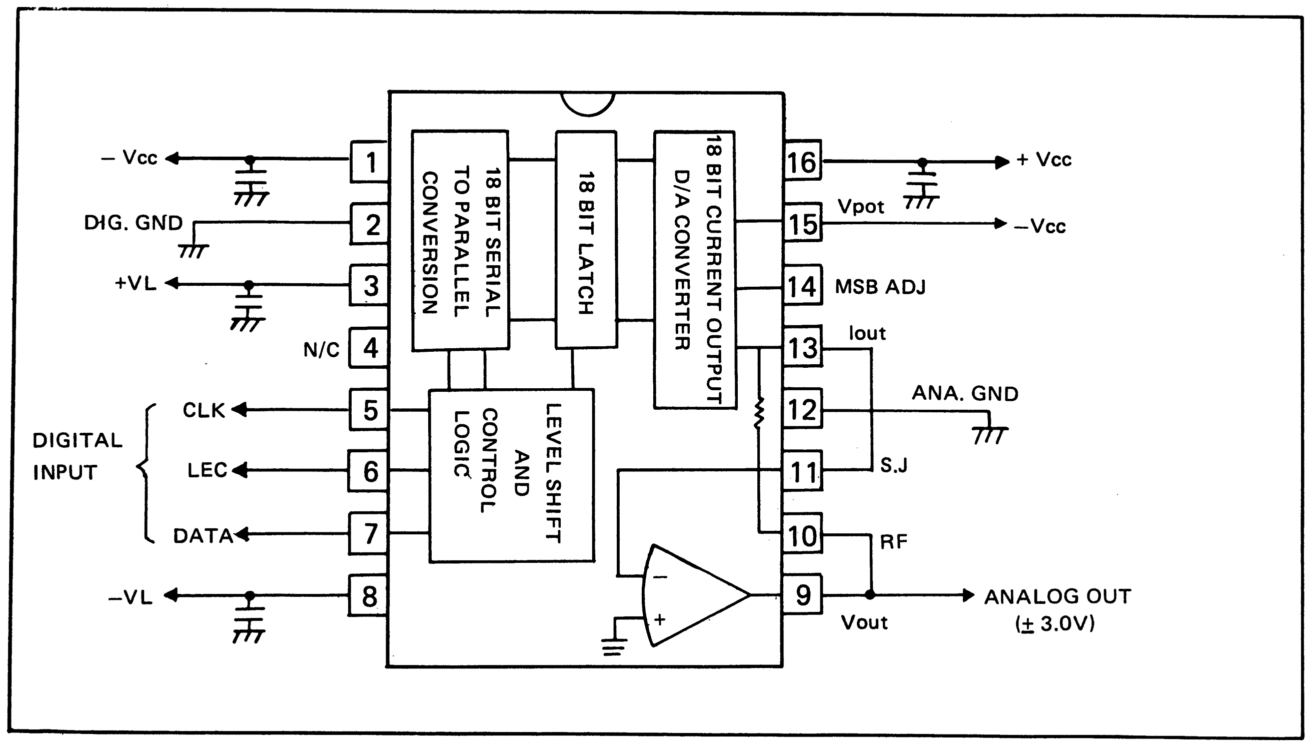
15-7. LC7582(LCD DRIVER) : UIC2


COM1
COM2
DATA
CLK
CE
V_{SS}
V_{LCD}
INH
V_{DD}
OSC
S53(ADO5)
S52(ADO4)
S51(ADO3)
S50(ADO2)
S49(ADO1)
S48(DSP OUT)
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
OPEN
S24
S25
S26
S27
S28
S29
S30
S31
S32
S33
S34
S35
S36
S37
S38
S39
S40
S41
S42
S43
S44(DSP2)
S45(AD2)
S46(DSP1)
S47(AD)
LC7582

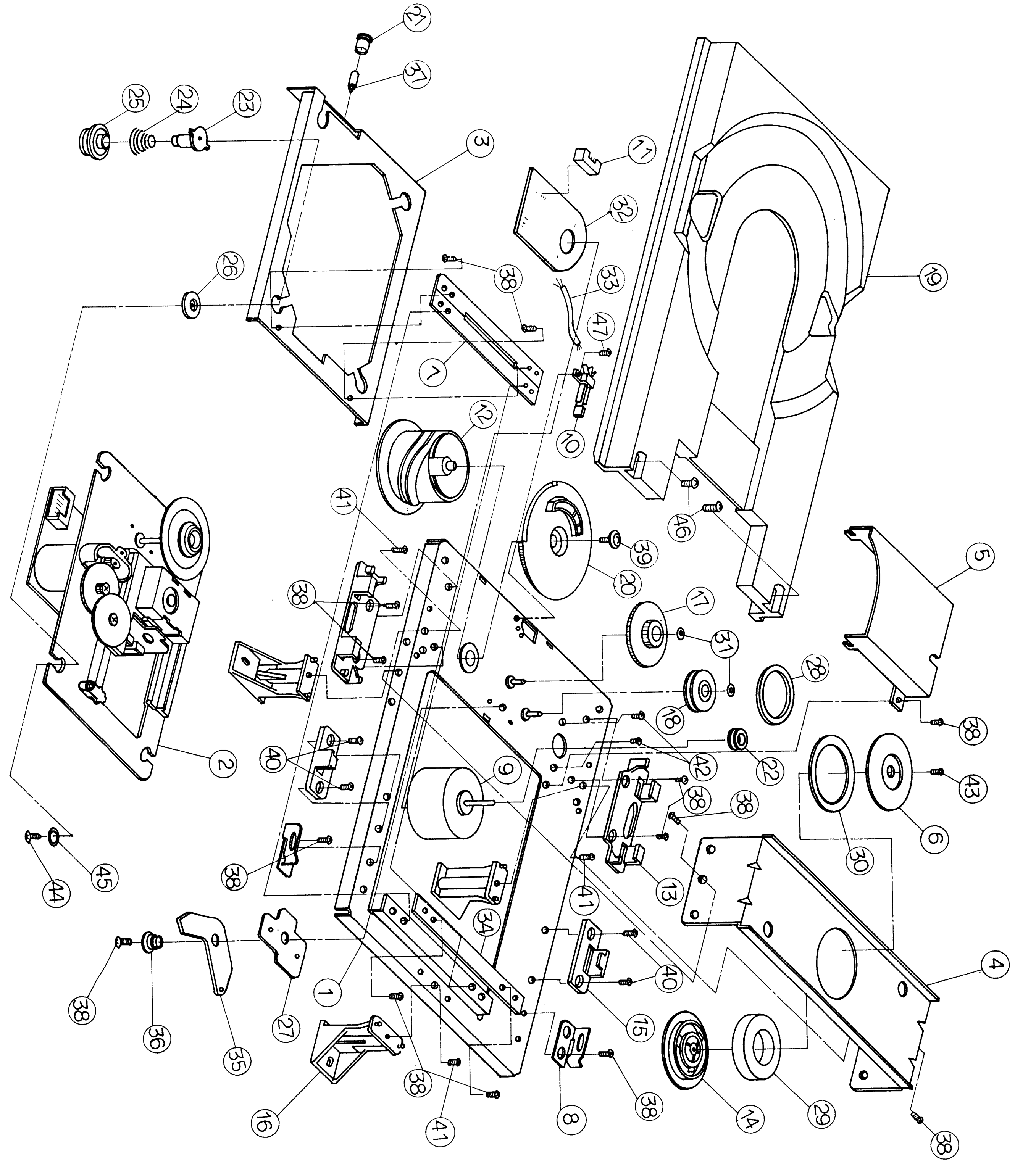
15-8. LC66508(MICOM) : UIC1


1 LINE MUTG
2 CLK
3 DATA
4 CE
5 REMOCON IN
6 G
7 POWER OFF
8 OSC CUT
9 LDON
10 FOK
11 SENS
12 GFS
13 CLK
14 XLT
15 DATA
16 XRST
17 SUBQ
18 CRCF
19 SQCK
20 EMP
21 DATA
22 CLOCK
23 CE
24 INH
25
26
27
28
29 SCOR
30 TEST
31 GND
32 OSC1
+5 64
63
62
61
60
59
TRAY OUT 58
IN 57
56
CD SYNC 55
G 54
53
PD2 52
PD1 51
PD0 50
PC3 49
PC2 48
PC1 47
PC0 46
PB3 45
PB2 44
PB1 43
PB0 42
41
40
OPEN 39
CLOSE 38
OPTION1 37
OPTION2 36
G 35
RESET 34
OSC2 33
UIC1 LC66508

15-9. PCM61P/AD1860N(DAC) : ZIC2 L, R


– Vcc
DIG. GND
+VL
N/C
DIGITAL INPUT
CLK
LEC
DATA
–VL
1
2
3
4
5
6
7
8
18 BIT SERIAL TO PARALLEL CONVERSION
18 BIT LATCH
18 BIT CURRENT OUTPUT D/A CONVERTER
LEVEL SHIFT AND CONTROL LOGIC
16
15
14
13
12
11
10
9
+ Vcc
Vpot
–Vcc
MSB ADJ
Iout
ANA. GND
S.J
RF
Vout
ANALOG OUT
(± 3.0V)

16-2. CD DECK : MCD350 (14929-428-010)


21
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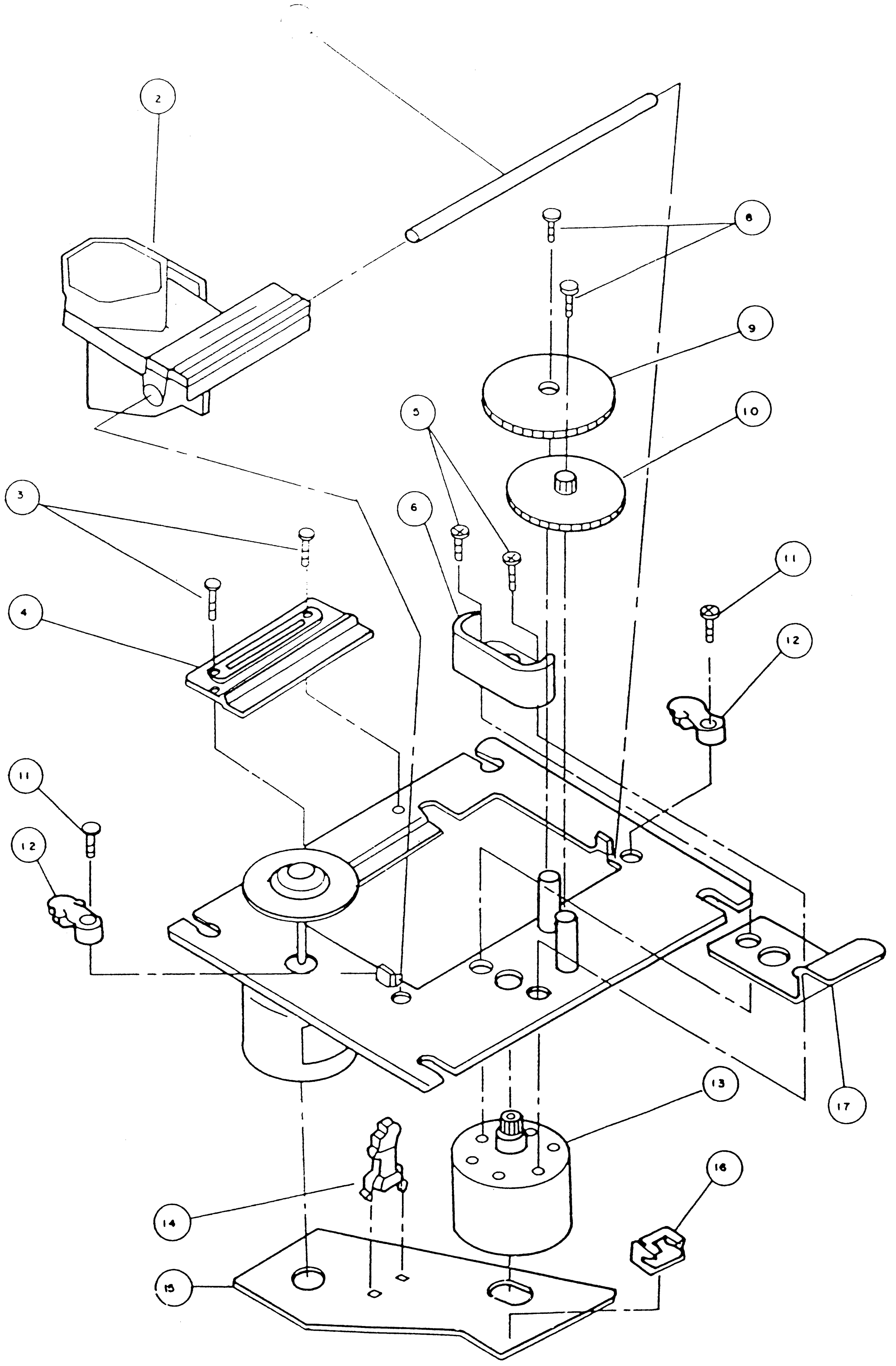
2

EXPLODED VIEW/PARTS LIST

- OPTICAL PICK-UP CARRIAGE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15

No.	Symbol	I/O	Description
41	RA04	O	Output address of external RAM. ADDR04
42	RA05	O	Output address of external RAM. ADDR05
43	RA06	O	Output address of external RAM. ADDR06
44	RA07	O	Output address of external RAM. ADDR07
45	RA08	O	Output address of external RAM. ADDR08
46	RA09	O	Output address of external RAM. ADDR09
47	RA10	O	Output address of external RAM. ADDR10
48	RA11	O	Output address of external RAM. ADDR11 (MSB)
49	RAWE	O	Writes enable output signal to external RAM. (Active when "L".)
50	RACS	O	Chip select output signal to external RAM. (Active when "L".)
51	C4M	O	Divider output for crystal. f = 4.2336MHz
52	Vss	–	GND (0V)
53	XTAI	I	Input to crystal oscillator circuit. Depending on the mode the frequency is either f = 8.4672 or 16.9344MHz.
54	XTAO	O	Output from crystal oscillator circuit. Depending on the mode the frequency is either f = 8.4672 or 16.9344MHz.
55	MD1	I	Mode selection input 1.
56	MD2	I	Mode selection input 2.
57	MD3	i	Mode selection input 3.
58	SLOB	I	Code switch input for audio data output. 2's complement output when "L", off set binary output when "H".
59	PSSL	O	Code switch input for audio data ouput. Serial output when "L", parallel output when "H".
60	APTR	O	Control output for aperture compensation. "H" during R-ch.
61	APTL	O	Control output for aperture compensation. "H" during L-ch.
62	DA01	O	DA01 (LSB of parallel audio data) is output when PSSL = "H". C1F1 is output when PSSL = "L".
63	DA02	O	DA02 is output when PSSL = "H". C1F2 is output when PSSL = "L".
64	DA03	O	DA03 is output when PSSL = "H". C2F1 is output when PSSL = "L".
65	DA04	O	DA04 is output when PSSL = "H". C2F2 is output when PSSL = "L".
66	DA05	O	DA05 is output when PSSL = "H". C2FL is output when PSSL = "L".
67	DA06	O	DA06 is output when PSSL = "H". C2PO is output when PSSL = "L".
68	DA07	O	DA07 is output when PSSL = "H". RFCK is output when PSSL = "L".
69	DA08	O	DA08 is output when PSSL = "H". WFCK is output when PSSL = "L".
70	DA09	O	DA09 is output when PSSL = "H". PLCK is output when PSSL = "L".
71	DA10	O	DA10 is output when PSSL = "H". UGFS is output when PSSL = "L".
72	DA11	O	DA11 is output when PSSL = "H". GTOP is output when PSSL = "L".
73	VDD	–	Power supply (+5V)
74	DA12	O	DA12 is output when PSSL = "H". RAOV is output when PSSL = "L".
75	DA13	O	DA13 is output when PSSL = "H". C4LR is output when PSSL = "L".
76	DA14	O	DA14 is output when PSSL = "H". C2IO is output when PSSL = "L".
77	DA15	O	DA15 is output when PSSL = "H". C2IO is output when PSSL = "L".
78	DA16	O	DA16 (MSB of parallel audio data) is output when PSSL = "H". DATA is output when PSSL = "L".
79	WDCK	O	Strobe signal output. Output is 176.4KHz when DF is on. Output is 88.2KHz when DF is off or when the chip being used is CXD1125Q.
80	LRCK	O	Strobe signal output. Output is 88.2KHz when DF is on. Output is 44.1KHz when DF is off or when the chip being used is CXD1125Q.

Notes)

C1F1: C1F2:	Monitor output reporting status of error correction for C1 decoder.
C2F1: C2F2:	Monitor output reporting status of error correction for C2 decoder.
C2FL:	Output of status condition. C2FL is set "H" when the C2 sequence presently being corrected becomes impossible to correct.
C2PO:	Display output of the C2 pointer. It is synchronized with the audio data output.
RECK:	Read frame clock output. 7.35KHz of the crystal system.
$\overline{\text{WFCK}}$:	Write frame clock output. 7.35KHz when locked by the crystal system.
$\overline{\text{PLCK}}$:	Output VCO/2. f = 4.3218MHz when locked by the EFM signal.
UGES:	Output for unprotected frame sync patterns.
GTOP:	Output for display of status of frame sync protection.
RAOV:	Output for display of either RAM overflow or underflow for ±4 frame jitter absorption.
C4LR:	Strobe signal. 352.8KHz when DF is on, 176.4KHz when DF is off, or when the LSI is CXD1125Q.
$\overline{\text{C21O}}$:	Inverse output of C210.
C21O:	Bit clock output. 4.2336MHz when DF is on, 2.1168MHz when DF is off, or when the LSI is CXD1125Q.
DATA :	Serial data output of audio signal.